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Low-frequency noise measurements on submicrometre n-channel and p-channel MOSFETs at various operating regions

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Silicon founders give in their MOS transistor card models some low-frequency noise parameters for SPICE-based circuit simulators corresponding to pure $1/f^a$ or flicker noise, with a very close to unity. MOS transistors used in analogue circuit applications are usually devices with large channel length and width. In low-noise applications, methods such as correlated double sampling are used to suppress the low frequency noise generated by them. Nevertheless, the transistors presently are submicrometre devices exhibiting very different low-frequency noise behaviour. In this paper, experimental low-frequency noise results obtained at room temperature on NMOS and PMOS transistors fabricated using a 0.7 μm process are presented. Both large and small devices on the same process are considered. All regions of operation of transistors are considered. We show that the low-frequency noise behaviour of small area MOSFETs is very different from that of large area devices and that the spectrum is the summation of Lorentzian spectra generated by the switching of individual active traps.

1. Introduction

CMOS image sensors designed using standard CMOS technologies offer some advantages compared with charge coupled devices (CCDs), such as lower power consumption, lower cost, compatibility with integration on-chip electronics and random access of the image data, and are used now in many applications including multimedia, space applications, industrial vision, etc. (Fossum 1997, Cavadore *et al.* 1998, Değerli *et al.* 2000).

The transistors used in analogue circuit applications are often large-area devices. Nevertheless, in CMOS image sensors, the use of very large devices is not possible owing to the pixel fill-factor and responsivity (μV/e) constraints. Moreover, the CMOS technologies used nowadays are often submicrometre MOS processes with short transistor channel lengths ($L < 1\,\mu m$). The impact of device scaling down on the performance of future CMOS image sensors has been studied recently (Wong 1996). In high-precision applications, the noise limits the dynamic range of the CMOS image sensors. The $1/f$ noise generated by the MOS transistors used in read-out circuitry is suppressed using correlated double-sampling techniques (Yadid-Pecht *et al.* 1997, Değerli *et al.* 2000). One of the major problems of scaling down is the change in the low-frequency noise behaviour of the MOS transistors. In Wong (1996) there is very little information about the low-frequency noise behaviour of

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scaled-down CMOS image sensors. In the present paper, we focus on this issue. After a brief theoretical background, we present measurements of the drain current noise spectral density S_{Id} for process test transistors available on every wafer of a fabrication run. Gate biases V_{GS} extend from 0.6 V to 5 V and drain biases V_{DS} from 0.1 V to 5 V. This allows us to analyse the noise behaviour for the characteristic biases: weak, moderate and strong inversion, linear and nonlinear region. Both n-channel and p-channel large area and small area devices fabricated using the same submicrometre process are considered.

2. Low-frequency noise in MOSFETs

The low-frequency noise in semiconductor devices has been studied for more than four decades (Claeys and Simoen 1997) but the origins of the low-frequency noise in MOS transistors are not really well understood. There are several noise models proposed in literature, considering all operating regions and inversion levels. However, most of them are valid only for long-channel devices and need physical parameters rarely provided by silicon founders.

In the carrier number fluctuations (ΔN) model, as originally proposed by McWhorter (1957), the $1/f$ noise is attributed to the random trapping and detrapping processes of charges in the oxide traps near the $Si–SiO_2$ interface. The charge fluctuations result in fluctuations of the surface potential, which in turn modulate the channel mobile carrier density. It is assumed that the channel can exchange charges with the interfacial oxide traps through tunnelling. The mobility fluctuations ($\Delta\mu$) model, on the other hand, considers that the $1/f$ noise results from the fluctuations of bulk mobility on the basis on an empirical hypothesis proposed by Hooge (1976, 1994). This subject is still open to debate between these two models (Simoen and

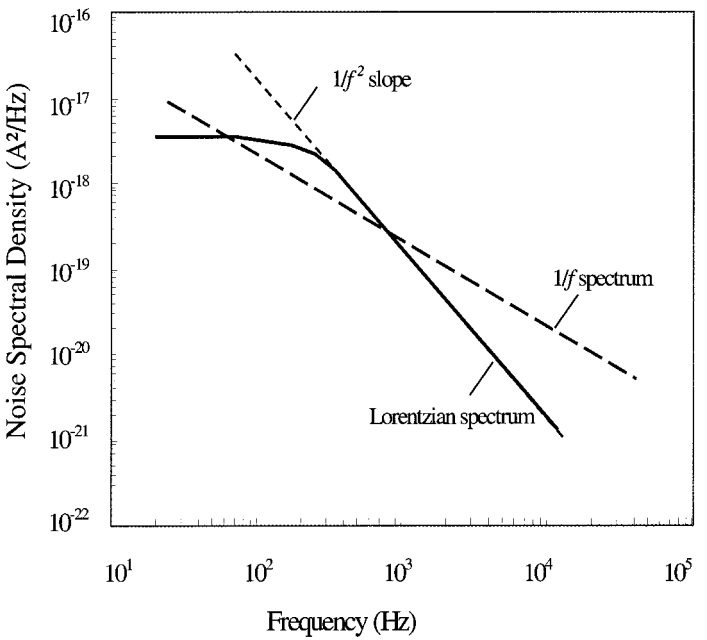


Figure 1. Comparison of a $1/f$ noise spectrum and a Lorentzian spectrum.

Claeys 1999). Extensive but sometimes inconsistent low-frequency noise data for MOSFETs have been reported, and neither of these two models explains all the experimental results reported in the literature. The low-frequency noise behaviour of the MOS transistor depends strongly on the processes used. Also, very different low-frequency noise behaviours for NMOS and PMOS have been observed.

Recently, substantial new insights into the $1/f$ problem have been obtained through the study of the noise properties of small area devices (Tsai and Ma 1994). For MOSFETs with very small channel area ($< 1\,\mu m^2$), it is possible to have only a single active oxide trap in the vicinity of the quasi-Fermi level over the entire channel. Capture and emission of a channel carrier by the trap result in discrete modulation on the channel current, resulting in a random telegraph signal (RTS) (Simoen *et al.* 1992) with a Lorentzian spectrum (figure 1). For large-area devices, the superposition of these individual RTSs, from all the traps in the oxide layers near the surfaces of the device, results in $1/f$ noise. The random switching between two discrete levels of the drain current has generally been modelled as the superposition of both the effect of the fluctuation in the number of free carriers, and the mobility fluctuation that occurs when the trap changes its state (Hung *et al.* 1990, Shi *et al.* 1994).

3. Experimental set-up

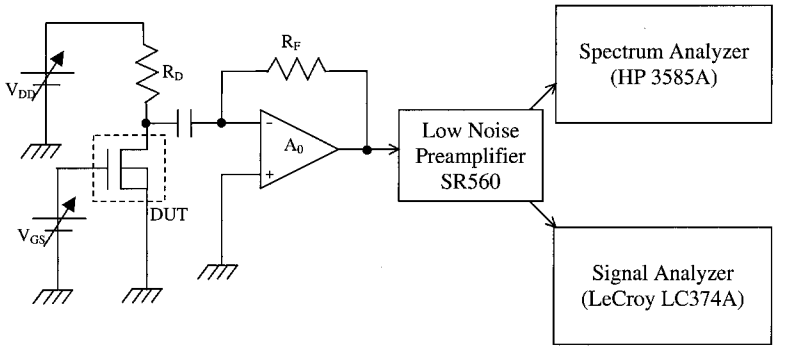
The submicrometre devices used in this study were fabricated using an Alcatel Microelectronics 0.7 μm CMOS technology. The threshold voltage values given in card models are $V_{th} = 0.76\,V$ for n-channel transistors and $V_{th} = -1.0\,V$ for p-channel transistors. The oxide thickness is $T_{OX} = 175\,Å$.

Figure 2(*a*) shows the schematic of a system developed for the measurement of the drain current noise spectra. The noise in the drain current is detected by a low-noise current preamplifier based on an LT1007 operational amplifier and the amplified noise signal is fed into an HP3585A spectrum analyser. The time domain signal is observed using a LeCroy LC374A digitizing scope. The gate and drain biases are provided by batteries V_{GS} and V_{DD} respectively. The substrate and the source of the MOSFET under test are connected to the system ground. The whole system is located in a Faraday cage, and all measurements are made at room temperature. Typical values for feedback resistance R_f are 10–100 kΩ. A small capacitance (5 pF) is connected across R_f to prevent A_0 from undergoing self-oscillation. Noise has been studied in the 100 Hz–100 kHz frequency bandwidth on p- and n-channel MOS transistors. The dc drain bias current of the test devices is measured using a Keithley 485 pico-amperemeter.

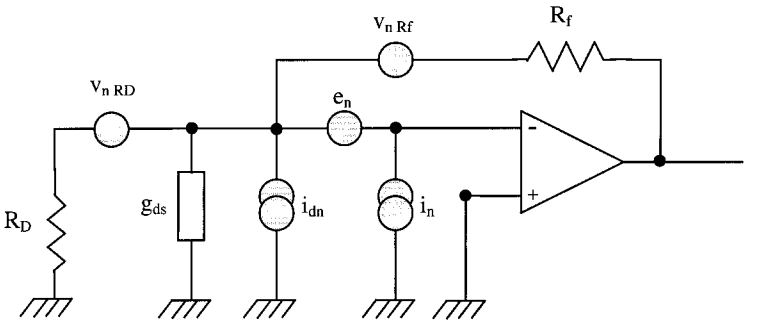
In most cases the drain current noise of the test MOSFET is much larger than the background noise of the measurement system. Nevertheless, it is straightforward to correct for the background noise if one desires. Figure 2(*b*) shows the equivalent circuit of the system. The noise power at the output of the low-noise preamplifier can be expressed as

$$\overline{\nu_n^2} = R_f^2(\overline{i_{dn}^2} + \overline{i_n^2}) + \left[1 + R_f\left(g_{ds} + \frac{1}{R_D}\right)\right]^2 \overline{e_n^2} + \overline{\nu_{nR_f}^2} + \overline{\nu_{nR_D}^2} \qquad (1)$$

where e_n and i_n are, respectively, the equivalent input noise voltage and noise current of the operational amplifier; i_{dn} is the noise drain current and g_{ds} is the MOSFET channel conductance. Terms ν_{nR_f} and ν_{nR_D} represent, respectively, the thermal noise in the feedback resistance R_f and in the drain bias resistance R_D.



(a)



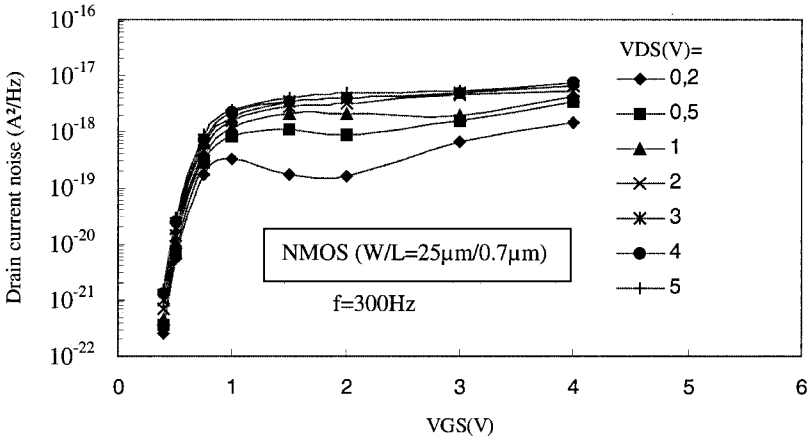
(b)

Figure 2. (*a*) Experimental set-up to measure the drain current noise. (*b*) The equivalent circuit for noise calculation.

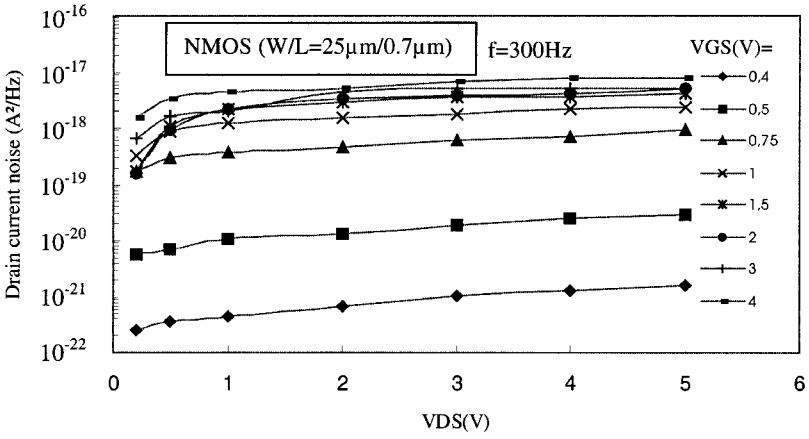
4. Experimental results and discussion

In this section we shall present typical measurement results. Figure 3(*a*) shows the bias dependence of drain current noise power at frequency $f = 300\,Hz$ for an n-channel MOSFET with $W \times L = 25\,\mu m \times 0.7\,\mu m$. For this device, the characteristics are quite regular. The drain current noise power increases with the gate voltage in weak and moderate inversion and tends to saturate in strong inversion. The measured drain current values are $I_D = 610\,nA$ for $V_{GS} = 0.4\,V$, $V_{DS} = 0.2\,V$; and $I_D = 1.36\,\mu A$ for $V_{GS} = 0.4\,V$, $V_{DS} = 4\,V$. The same data are plotted in a different manner in figure 3(*b*) to display more clearly the bias dependence of the noise power in the subthreshold region. In the linear region, the drain current noise power increases with increased drain bias, and then, in the non-ohmic region, increases slightly. Similar results were observed on other transistors with the same dimensions, fabricated on the same wafer.

The drain current noise of a p-channel MOSFET with the same dimensions ($W \times L = 25\,\mu m \times 0.7\,\mu m$) at frequency $f = 100\,Hz$ with various biases is reported in figure 4. We observe that the noise power is strongly dependent on drain bias above all subthreshold regions. The measured drain current values are $I_D = -50\,nA$



(a)



(b)

Figure 3. (*a*) Bias dependence of the drain current noise power of an NMOS ($W/L = 25\,\mu m/0.7\,\mu m$) fabricated by a submicrometre process ($f = 300\,Hz$). (*b*) The same data plotted in a different manner.

for $V_{GS} = -0.95\,V$, $V_{DS} = -0.2\,V$; and $I_D = -440\,nA$ for $V_{GS} = -0.95\,V$, $V_{DS} = -4\,V$. From figures 3 and 4, one observes that for a given gate and drain bias the n-channel MOSFETs are more noisy. In general, p-channel devices have noise levels lower than those of n-channel devices with similar gate geometry. This can be attributed to the larger tunnelling barrier experienced by holes across the Si–SiO_2 interface relative to that of electrons, and the different oxide trap densities near the valence and conductance band edges, as well as the different μ_n and μ_p, resulting in different degrees of surface mobility fluctuation.

Figure 5 shows the measurement results of the drain current noise characteristics in the strong inversion as well as subthreshold regions for a narrow p-channel MOSFET with $W \times L = 1\,\mu m \times 0.7\,\mu m$. For $V_{DS} = -0.2\,V$, some drain current

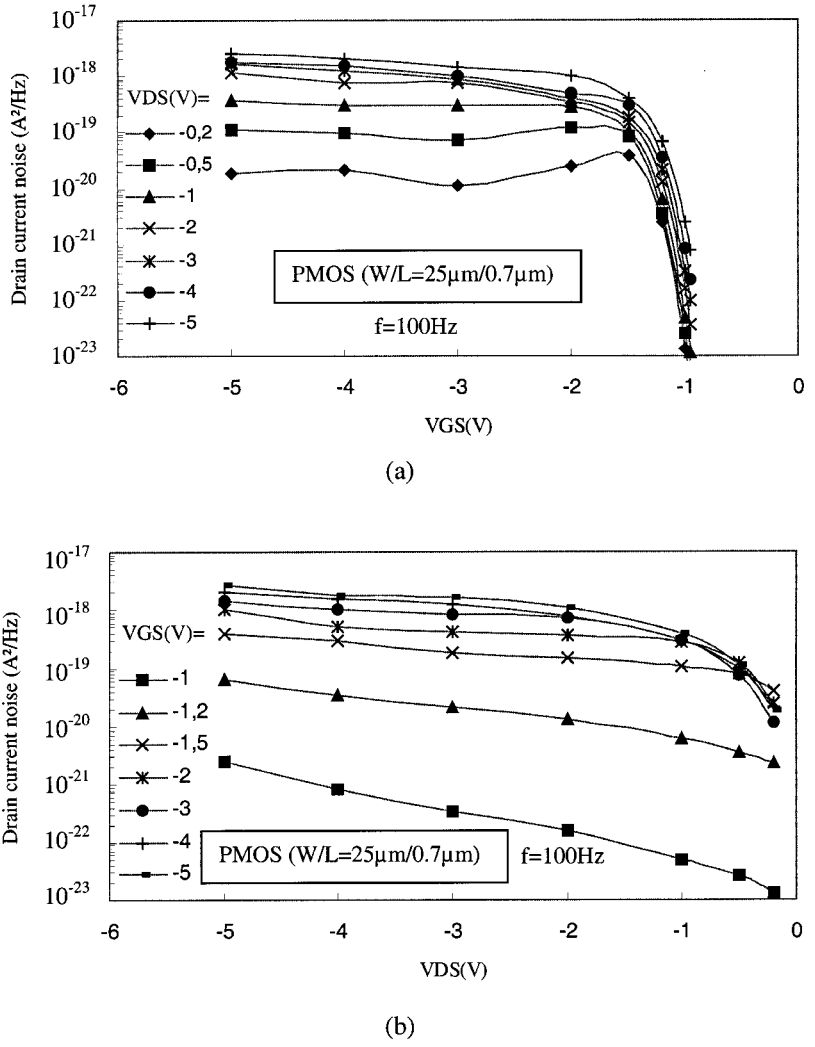


Figure 4. (*a*) Bias dependence of the drain current noise power of a PMOS ($W/L = 25\,\mu m/0.7\,\mu m$) fabricated by a submicrometre process ($f = 100$ Hz). (*b*) The same data plotted in a different manner.

values are as follows: $I_D = -21$ nA for $V_{GS} = -1.1$ V; $I_D = -226$ nA for $V_{GS} = -1.25$ V; $I_D = -1.31\,\mu A$ for $V_{GS} = -1.5$ V; and $I_D = -9.84\,\mu A$ for $V_{GS} = -3.0$ V. The channel width effects on the noise characteristics are evident through the comparison of figures 5 and 4. In contrast to the results obtained for the large p-channel device, for this device drain current noise power continues to increase with the gate voltage in both weak and strong inversion.

The bias dependence of the drain current noise power, measured at 300 Hz, of a small n-channel MOSFET ($W \times L = 1\,\mu m \times 0.7\,\mu m$) is presented in figure 6. We observe that in both weak and strong inversion levels the drain current noise power increases significantly with gate bias in both linear and nonlinear regions. We can also remark that the current noise is a weak function of the drain bias in the

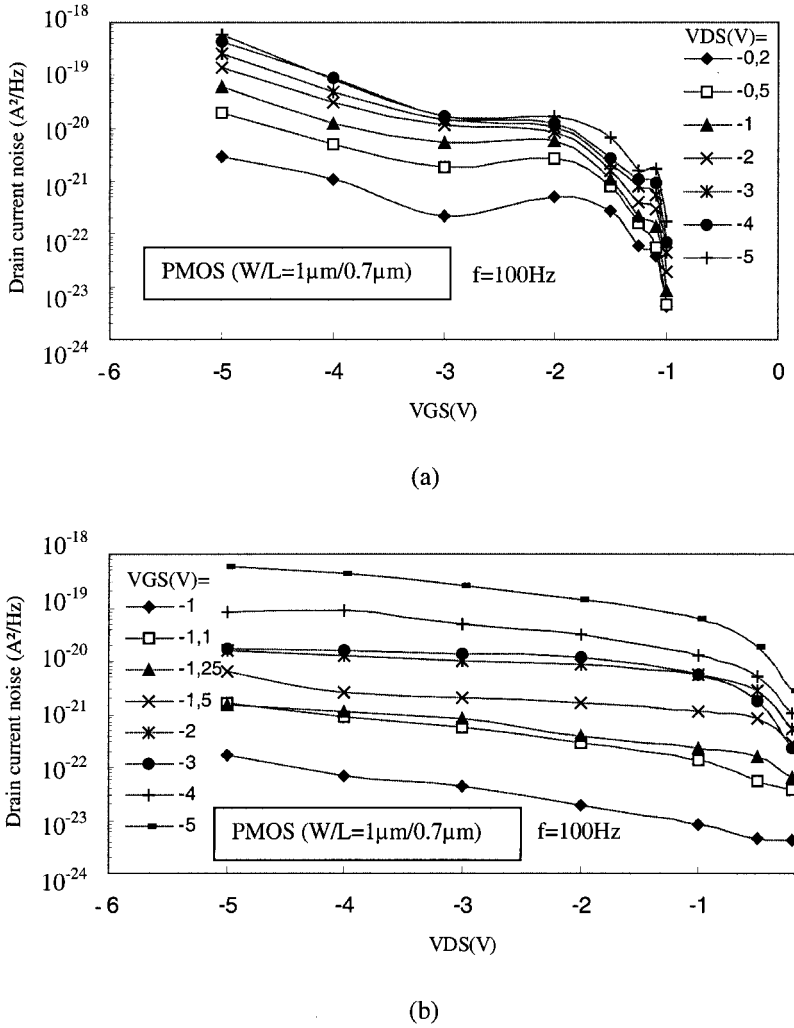


Figure 5. (*a*) Bias dependence of the drain current noise power of a small PMOS ($W/L = 1\,\mu m/0.7\,\mu m$) ($f = 100$ Hz). (*b*) The same data plotted in a different manner.

saturation region. The measured drain current values are as follows ($V_{DS} = 0.2$ V): $I_D = 126$ nA for $V_{GS} = 0.55$ V; $I_D = 302$ nA for $V_{GS} = 0.65$ V; $I_D = 543$ nA for $V_{GS} = 0.75$ V; $I_D = 1.43\,\mu A$ for $V_{GS} = 1.0$ V; $I_D = 4.90\,\mu A$ for $V_{GS} = 1.5$ V; and $I_D = 11.01\,\mu A$ for $V_{GS} = 2.0$ V.

Figure 7 shows the evolution of the drain current noise spectra for the same device in linear ($V_{DS} = 0.25$ V) and saturation ($V_{DS} = 4$ V) regions from weak inversion to strong inversion. At $V_{GS} = 4$ V, owing to the great number of active traps, the spectra are $1/f$ like. As the gate bias is decreased, the number of RTSs reduces and the spectra clearly exhibit the presence of a finite number of elementary Lorentzians. This is more evident from the time domain drain current fluctuations of the same device observed at $V_{GS} = 0.75$ V, $V_{DS} = 0.1$ V (figure 8). One observes few levels of RTSs with different times between jumps. In other words, there exist two or three active interface traps with different characteristic times and/or different

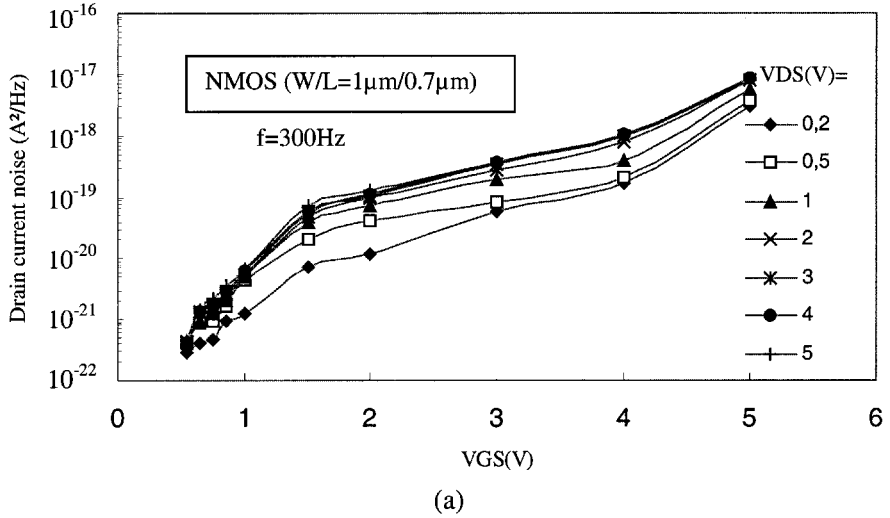
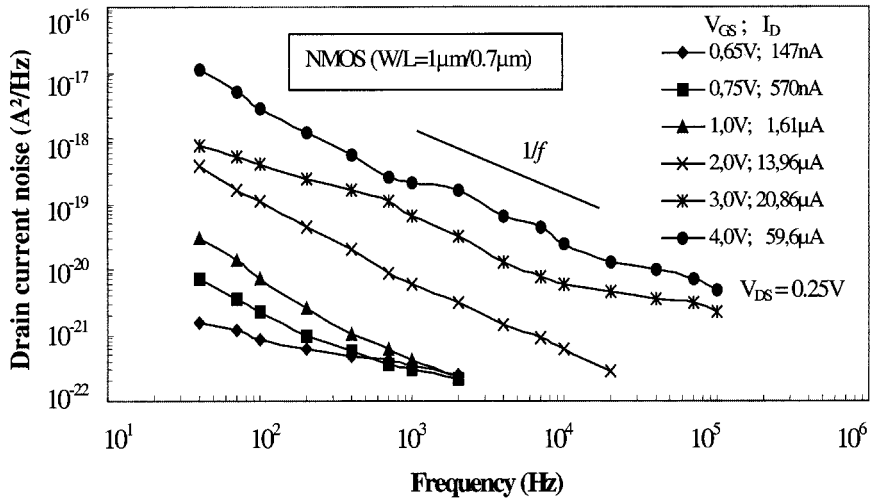


Figure 6. (*a*) Bias dependence of the drain current noise power of a small NMOS ($W/L = 1\,\mu m/0.7\,\mu m$) ($f = 300$ Hz). (*b*) The same data plotted in a different manner.

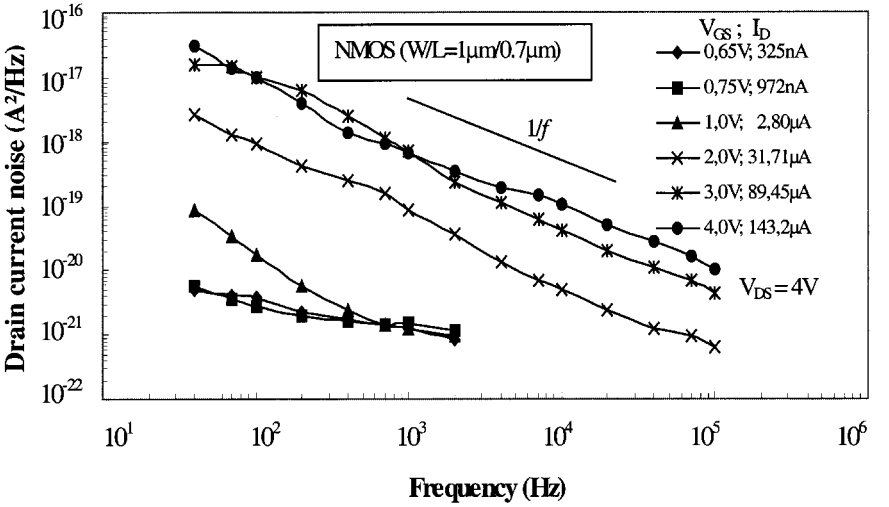
activation energies. Inspection of figures 7 and 8 shows that the spectrum of the device should then consist of the sum of a few individual Lorentzians.

5. Conclusion

We have carried out an experimental study of the noise current exhibited by submicrometre MOSFETs in both the ohmic and the non-ohmic region, operating at room temperature. It has been shown that $1/f^a$ noise spectra in small-area MOSFETs are the result of a superposition of random telegraph signals due to individual carrier events. Thus, of the competing views on the origins of $1/f^a$



(a)



(b)

Figure 7. Drain current noise power spectra for the NMOS (W /L = 1 μm/0.7 μm): (*a*) $V_{DS} = 0.25$ V (linear region); (*b*) $V_{DS} = 4$ V (saturation region).

noise in MOSFETs, namely, carrier trapping and mobility fluctuations, it is now clear that carrier trapping into states in the oxide drives the $1/f^a$ noise process. The role of interface states in producing RTSs and $1/f^a$ noise will become more important as we move toward technologies of low power dissipation applications and scaling down of the device dimensions.

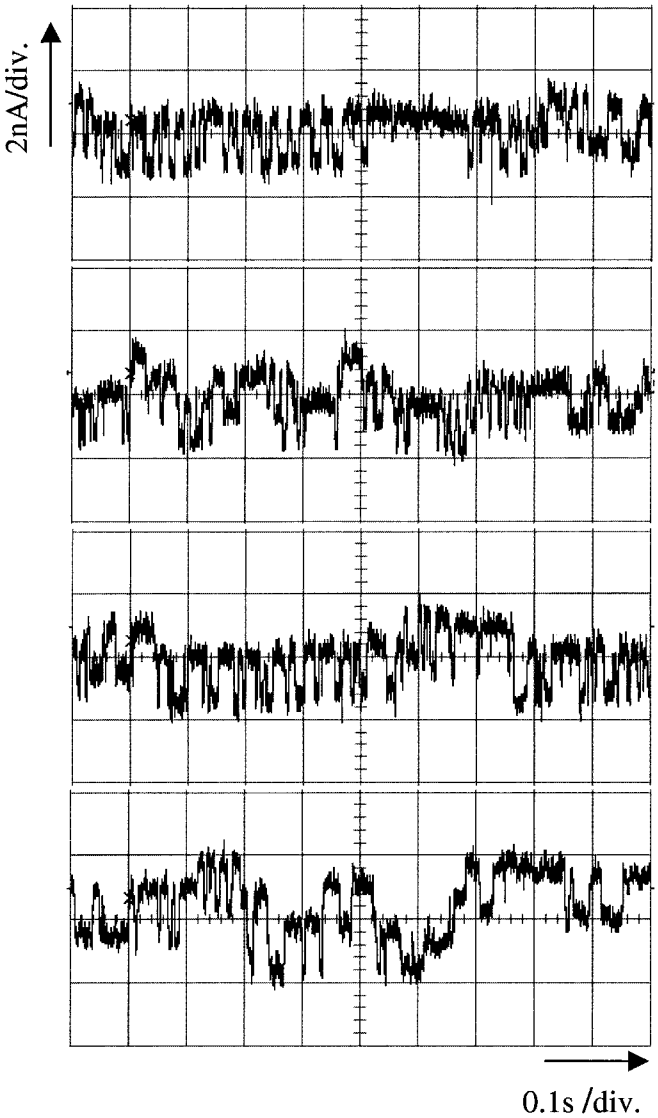


Figure 8. Time domain drain current fluctuations observed for an NMOS with $W/L = 1\,\mu m/0.7\,\mu m$ ($V_{GS} = 0.75\,V$, $V_{DS} = 100\,mV$, $I_D = 395\,nA$).

It should be pointed out that the spectrum of an individual RTS is 'white'. With regard to CMOS imagers, the device scaling will reduce the effectiveness of correlated double sampling circuits.

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