Analysis and Reduction of Signal Readout Circuitry Temporal Noise in CMOS Image Sensors for Low-Light Levels

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***Abstract*—In this paper, analytical noise analysis of correlated double sampling (CDS) readout circuits used in CMOS active pixel image sensors is presented. Both low-frequency noise and thermal noise are considered. The results allow the computation of the output rms noise versus MOS transistor dimensions with the help of SPICE-based circuit simulators. The reset noise, the influence of floating diffusion capacitance on output noise and the detector charge-to-voltage conversion gain are also considered. Test circuits were fabricated using a standard 0.7 μm CMOS process to validate the results. The analytical noise analysis in this paper emphasizes the computation of the output variance, and not the output noise spectrum, as more suitable to CDS operation. The theoretical results are compared with the experimental data.**

***Index Terms*—Active pixel sensors, CDS, CMOS image sensors, noise.**

I. Introduction

NOWADAYS, CMOS imagers compete with CCD's for low cost, and low power applications, but they suffer from the presence of noise [1], [2], a major drawback of the MOS transistors. To increase the dynamic range of a sensor, one would like to increase the maximum acceptable amplitude of the signal and to reduce the noise level. Thus, one way to enlarge the dynamic range of a sensor is to reduce the noise level.

The CMOS active pixel sensor readout circuit investigated in this paper is shown in Fig. 1(a), with related timing in Fig. 1(b) for photogate type pixels. This circuit is frequently used in various studies [3], [4]. It includes an in-pixel NMOS buffer (M_1–M_3), and a column circuitry consisting of two sampling capacitors ($C_{\rm ref}$ and $C_{\rm sig}$) and two PMOS buffers. M_1, M_5 and M_5' are source followers, while M_3, M_7, M_7' are load transistors. M_3 is common to all pixels of a column while M_7, M_7' are common to all columns. V_{LN} and V_{LP} sources determine the bias currents of the buffers. M_2 and M_6–M_6' are respectively pixel and column selection transistors.

The readout sequence unfolds as follows:

1) reset of the sense node by activating $M_{\rm RST}$;
2) sample of the reference level $V_{\rm ref}$ on the capacitor $C_{\rm ref}$;
3) transfer of the photonic charges into C_{fd} by turning-off PG;
4) sample of the signal level on $C_{\rm sig}$.

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Then, a differential readout is made by setting the column buffers active.

It should be pointed out that the readout sequence is slightly different for the standard three transistors photodiode type pixels [2], [3] which do not allow a real CDS operation, the signal level being sampled before the reference level. However, this mode of operation do not change anything in the theoretical analysis presented here. C_{fd} in that case represents mostly the capacitance of the photodiode.

Some hand analysis of noise for CMOS imagers are presented in literature [5], [6], but the MOS transistor noise models used in these studies are limited to long-channel devices. Moreover, the CDS operation essential for low-noise applications in CCD's [7] or CMOS image sensors, is not considered in these papers.

Nowadays, most of CMOS technologies use short channel MOS transistors ($L < 1$ μm) and it is well known that the low-frequency noise of MOS transistors increases as the channel length decreases [8]. The low-frequency noise performances become much important. The main difficulty in the noise analysis of CMOS imagers comes from the unavailability of simple MOSFET noise models, valid for all operating regions, especially for flicker noise.

The origins of the low-frequency noise in MOS transistors are not well understood and a debate is open between two models:

1) The McWhorter's carrier-number fluctuation (ΔN) model [9] which assumes that that the $1/f$ noise is caused by the random trapping and detrapping of the mobile carriers in the traps located at Si-SiO_2 interface and within the gate oxide, giving an input referred $1/f$ noise independent of the gate bias;
2) The Hooge's carrier-number fluctuation $(\Delta\mu)$ model [10] which considers the flicker noise as a result of the fluctuations in bulk mobility, giving an input referred low-frequency noise strongly dependant on the gate bias (see for example, [11], [12]).

Extensive but sometimes inconsistent low-frequency noise data for MOSFET's have been reported, and none of these two models explain all of experimental results reported in literature. The low-frequency noise behavior of the MOS transistor depends strongly on the process used.

In modern MOS transistors with very small geometries, only one active Si-SiO_2 interface trap may exist, giving birth of the so-called *random telegraph signals* (RTS) noise. Then, the low-frequency noise spectra of such transistors are often Lorentzian type (see for example, [13], [14]). The random switching between two discrete levels of the drain current, have generally

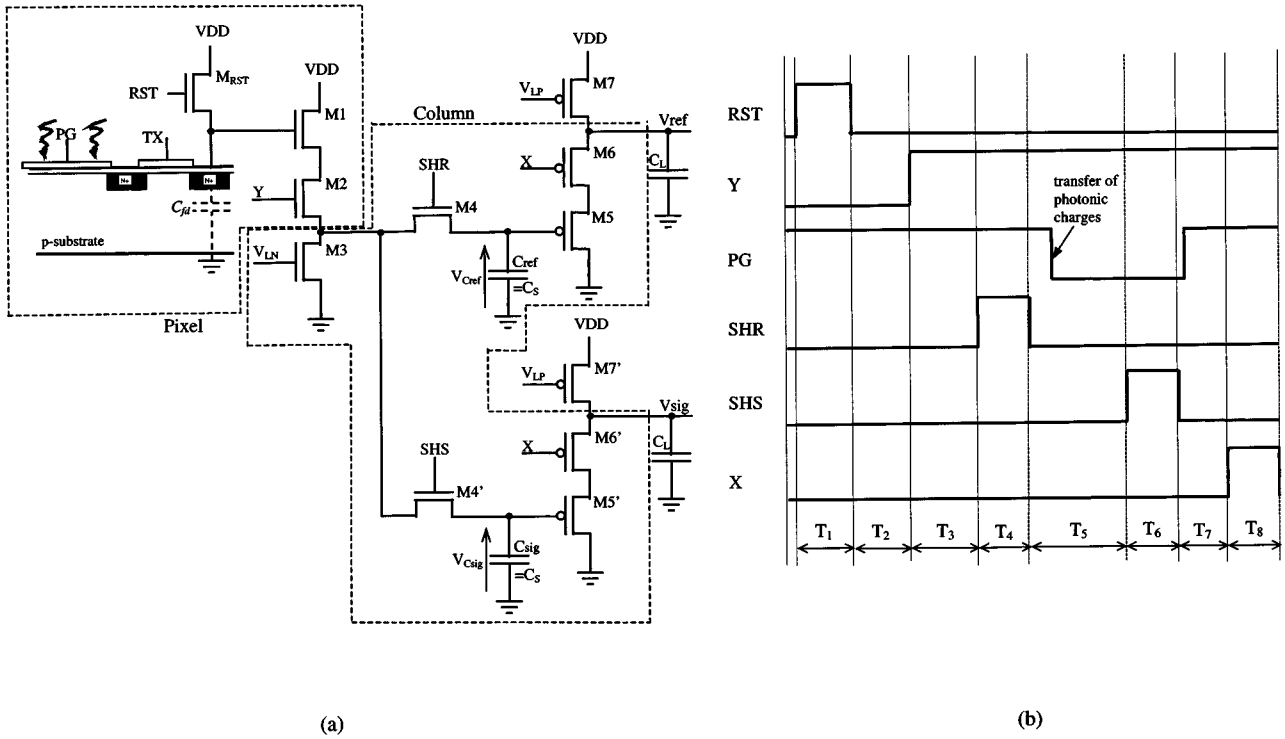


Fig. 1. (a) Readout circuit of CMOS photogate active pixel image sensor, and (b) related timing.

been modeled as the superposition of both the effect of fluctuation in the number of free carriers, and the mobility fluctuation that occur when the trap changes its state [8], [14], [15]. Reference [16] is a recent review paper on the low-frequency noise in MOSFET's.

Designers can take advantage of circuit simulator noise models to obtain the power spectral density (PSD) of the MOSFET noise sources, thanks to the process related noise parameters supplied in transistor models by silicon foundries. But as the output noise of the circuit is time-varying, the total output noise is the sum of the noise stored on capacitors at different times and SPICE-like simulators are usually not suitable for such noise analysis. So we developed analytical expressions for the total noise power of the readout circuit given in Fig. 1(a) from the small-signal equivalent circuit of the MOS transistor. By running dc SPICE simulations, the dc point information and the other parameters (transconductances, capacitances, voltages, currents, etc.) corresponding to different bias conditions or device geometries are determined, and these values are used to calculate the thermal and flicker noise spectral densities for each transistor. This method appears as a practical solution for helping the design of CMOS imagers to analyze the noise behavior.

It should be noted that, in this study, the noise in steady-state condition only is considered, i.e., according to the practical operation of the CMOS active pixel sensor, at sampling instant, the signal and noise levels reach their stationary level or equilibrium. In other words, the signal and noise transients are ended and both signal and noise means are no more varying. Otherwise, the MOS transistor noise models used would not be usable and a nonstationary state variable method should be used [17]–[19].

Other noise sources, such as photon shot noise and dark current shot noise [4], are not considered in this paper.

In the next section, we will develop analytical expressions for the output noise power spectral densities of the in-pixel NMOS buffer and the column PMOS buffer, given in Fig. 1(a), as a function of the noise densities of the transistors. Then we will compute the total output variance of the circuit, with and without CDS operation, using these PSD's. In Section V, we will survey briefly the existing MOS transistor thermal and flicker noise models we will use in our readout circuit noise expressions. Finally, we will discuss the experimental and theoretical results in order to optimize the device geometries of the readout circuit, then the effect of various parameters on the output noise. Previous studies were conducted on CCD's in a quite similar way [20]; our work takes into account the $1/f$ noise and makes use of recent MOS transistor noise models implemented in circuit simulators, and suitable for the submicron technologies used for CMOS image sensors.

II. Analysis of the Total Output Noise PSD of the Buffers

The common small-signal equivalent circuit of the MOS transistor is shown in Fig. 2 [21]. The drain-source current, $I_{\rm ds}$, is the main contributor to the MOS behavior. For the ac and noise analysis, g_m gate transconductance, g_{mb} substrate transconductance, and $g_{\rm ds}$ drain-source conductance, which are the partial derivatives of $I_{\rm ds}$ with respect to the voltages $V_{\rm gs}, V_{\rm bs}$, and $V_{\rm ds}$ respectively, are used. The channel noise is represented by i_{nd}^2.

r_d and r_s are drain and source dynamic access resistances, respectively. These resistances contribute to the noise of the device. Their effect may become important for very short-channel

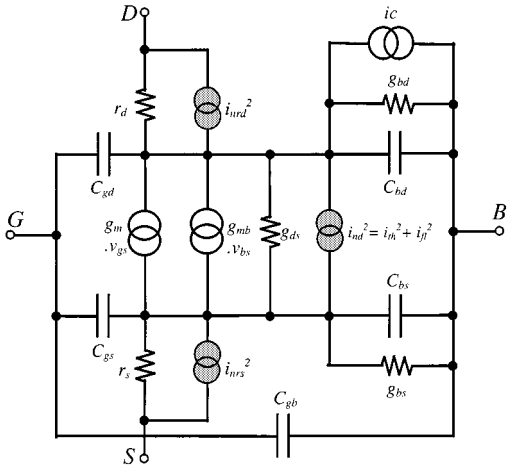


Fig. 2. Small signal equivalent circuit of the MOS transistor for the ac and noise analysis used actually in circuit simulators.

devices [22]. Modern processes make use of silicidation to lower their value, and their impact is reduced considerably [23].

In this equivalent circuit, ic is the bulk current caused by impact ionization effects. Its value depends on all terminal voltages. The parasitic static bulk diode effects are represented by the bulk-drain and bulk-source junction currents $I_{\rm bd}$ and $I_{\rm bs}$. The transconductances $g_{\rm bd}$ and $g_{\rm bs}$ are defined as

$$g_{\rm bd} = \frac{\partial I_{\rm bd}}{\partial V_{\rm bd}}, \quad g_{\rm bs} = \frac{\partial I_{\rm bs}}{\partial V_{\rm bs}}.$$

In circuit simulators, the noise contributions of $g_{\rm bd}, g_{\rm bs}$ and ic are usually neglected.

1) In-Pixel NMOS Buffer: The electrical equivalent circuit of the in-pixel NMOS buffer with the sampling capacitor at the sampling instant [T_4 in Fig. 1(b)] is given in Fig. 3(a). C_S represents the sampling capacitor [$C_{\rm ref}$ or $C_{\rm sig}$ in Fig. 1(a)]. C_{fd} is the sum of all the capacitances between the gate terminal of M_1 and the ground. The parasitic capacitances, such as poly/bulk, metal/n+, and metal/poly wiring and contact capacitances, are also included in C_{fd}. C_{gs1} is the gate-to-source capacitance of M_1. In this phase, C_{fd} is previously charged to an initial dc value $V_{Cfd}(0)$ via the transistor $M_{\rm RST}$.

As we consider only the stationary case, the gate terminals of the pixel selection transistor M_2 and the sampling transistor M_4 are held at logical "high" potential level, i.e., $V_{\rm DD}$. The transistors M_1 and M_3 operate in saturation region, and M_2 and M_4 in the linear region.

The small-signal equivalent circuit of the circuit is shown in Fig. 3(b) where i_n denotes i_{nd} and $R_3 = 1/g_{\rm ds3}$. The selection transistor M_2 and the sampling transistor M_4 are represented by their "ON" resistances ($r_2 = 1/g_{\rm ds2}, r_4 = 1/g_{\rm ds4}$), and their noise voltage sources by e_{n2} and e_{n4}, respectively ($e_{n2} = i_{n2} \cdot r_2$ and $e_{n4} = i_{n4} \cdot r_4$). For the sake of simplicity, the bulk-drain $(g_{\rm bd})$ and bulk-source $(g_{\rm bs})$ junction currents, the drain and source dynamic access resistances of the transistors are neglected. The $C_{\rm ds}$ and $C_{\rm sb}$ capacitances of M_1 are also neglected. In this case, the bulk and drain terminals of M_1 are "short-circuited."

Nevertheless, it should be pointed out that, to determine dc operating point information of the circuit, all parasitic effects such as, body effects of switches, bulk currents, etc., are considered by SPICE.

A nodal analysis in the frequency domain ($\omega = 2\pi f$) of the equivalent circuit of Fig. 3(b) leads to the relation for the output noise level (Appendix A)

$$v_N = \frac{R_{\rm eq1} i_{n1} + e_{n2} + (r_2 + R_3) i_{n3} + e_{n4}}{1 + j(\omega/\omega_{\rm eqn})} \tag{1}$$

with

$$R_{\rm eq1} = \left[g_{mb1} + g_{m1} \frac{C_{fd}}{C_{fd} + C_{gs1}} \right]^{-1} \quad \text{and}$$

$$\omega_{\rm eqn} = \left[C_S \left(r_4 + \frac{R_3 (R_{\rm eq1} + r_2)}{R_3 + R_{\rm eq1} + r_2} \right) \right]^{-1}$$

where $R_{\rm eq1}$ is the dynamic output resistance of M_1 seen from its source terminal.

Equation (1) may be rewritten as

$$v_N = H_1(\omega) \cdot i_{n1} + H_2(\omega) \cdot e_{n2} + H_3(\omega) \cdot i_{n3} + H_4(\omega) \cdot e_{n4}$$

where

$$H_1(\omega) = \frac{R_{\rm eq1}}{1 + j(\omega/\omega_{\rm eqn})}, \quad H_2(\omega) = \frac{1}{1 + j(\omega/\omega_{\rm eqn})},$$

$$H_3(\omega) = \frac{r_3 + R_3}{1 + j(\omega/\omega_{\rm eqn})} \quad \text{and} \quad H_4(\omega) = \frac{1}{1 + j(\omega/\omega_{\rm eqn})}.$$

As i_{n1}, e_{n2}, i_{n3}, and e_{n4} are the uncorrelated random inputs of a linear system having v_N as output, the total PSD is given by

$$S_{v_N} = |H_1(\omega)|^2 \cdot S_{i_{n1}} + |H_2(\omega)|^2 \cdot S_{e_{n2}} + |H_3(\omega)|^2 \cdot S_{i_{n3}} + |H_4(\omega)|^2 \cdot S_{e_{n4}} \tag{2}$$

where $S_{i_{n1}}, S_{e_{n2}}, S_{i_{n3}}$ and $S_{e_{n4}}$ denote the PSD of each corresponding input, constant for white noise and inversely proportional to the frequency for the $1/f$ noise. Thus, considering steady-state conditions, the total output noise PSD of the circuit on the capacitor C_S is given by

$$S_{v_N} = \frac{R_{\rm eq1}^2 S_{i_{n1}} + S_{e_{n2}} + (r_2 + R_{\rm eq1})^2 S_{i_{n3}} + S_{e_{n4}}}{1 + (\omega/\omega_{\rm eqn})^2} = \frac{R_{\rm eq1}^2 S_{i_{n1}} + r_2^2 S_{i_{n2}} + (r_2 + R_{\rm eq1})^2 S_{i_{n3}} + r_4^2 S_{i_{n4}}}{1 + (\omega/\omega_{\rm eqn})^2} \tag{3}$$

where i_{n2} and i_{n4} are the equivalent Norton current sources of e_{n2} and e_{n4}.

2) Column PMOS Buffer: The electrical equivalent circuit of the column PMOS buffer at the column read phase [T_8 in Fig. 1(b)] is given in Fig. 4(a) where C_L is the load capacitance, $r_6 = 1/g_{\rm ds6}$, and $R_7 = 1/g_{\rm ds7}$. The sampling capacitor C_S is previously charged to an initial dc value $V_S(0)$ via the transistor M_4. The buffer is activated by setting X "low." In this case, the $C_{\rm gs}$ capacitance of M_5 is very small compared to C_S. By using the same way as previously used for the NMOS buffer, one can find the total output noise PSD of the PMOS buffer as

$$S_{v_P} = \frac{R_{\rm eq2}^2 S_{i_{n5}} + S_{e_{n6}} + (r_6 + R_{\rm eq2})^2 S_{i_{n7}}}{1 + (\omega/\omega_{\rm eq1p})^2} = \frac{R_{\rm eq2}^2 S_{i_{n5}} + r_6^2 S_{i_{n6}} + (r_6 + R_{\rm eq2})^2 S_{i_{n7}}}{1 + (\omega/\omega_{\rm eq1p})^2} \tag{4}$$

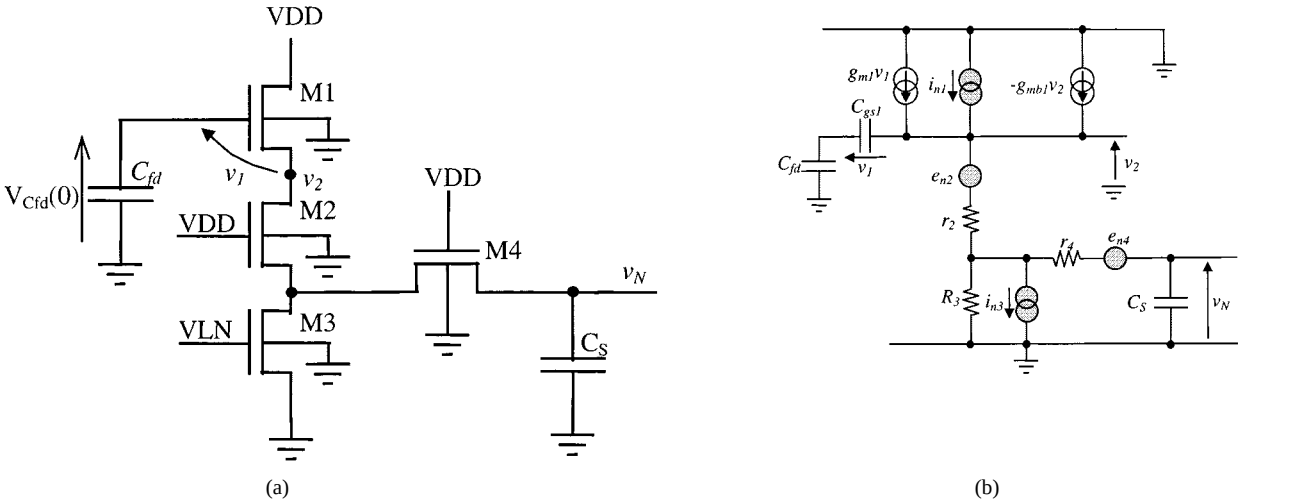


Fig. 3. (a) In-pixel NMOS buffer during the sampling phase, and (b) its small-signal equivalent circuit for noise analysis.

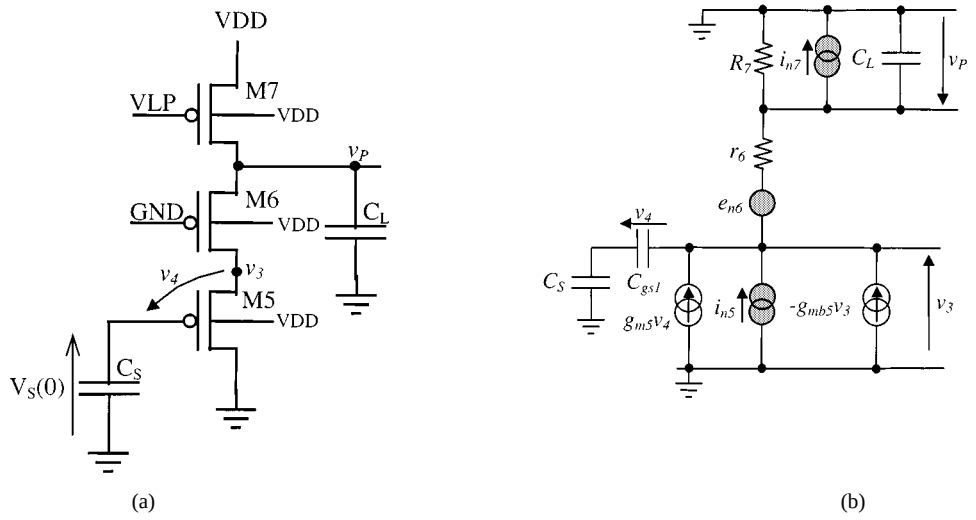


Fig. 4. (a) Column PMOS buffer during the sampling phase, and (b) its small-signal equivalent circuit.

with

$$R_{\text{eq2}} \approx [g_{mb5} + g_{m5}]^{-1}, \quad \text{and}$$
$$\omega_{\text{eq}p} = \left[\frac{C_L R_7 (R_{\text{eq2}} + r_6)}{R_7 + R_{\text{eq2}} + r_6}\right]^{-1}.$$

R_{eq2} is the dynamic output resistance of M_5 seen from its source terminal. The assumptions made in Appendix A for the NMOS buffer are also used for the PMOS buffer.

III. Analysis of the Output RMS Noise with CDS Operation

A. CDS Effect on the Output Variance

The equivalent block diagram of the CDS operation used to compute the output variance is illustrated in Fig. 5. The input reference signal and noise are stored on C_{ref} during the phase T_4. At the beginning of that phase, the initial voltage $v_{C_{\text{ref}}}(0)$ across this capacitor is statistically independent of the reference signal level. We assume that the filter reaches its steady-state

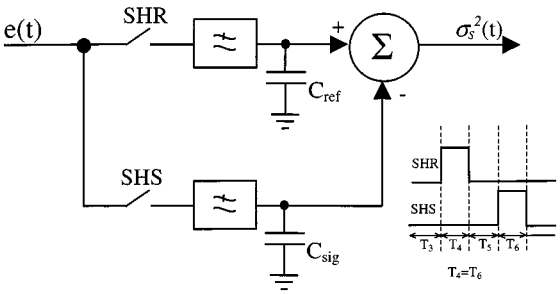


Fig. 5. Block diagram of the CDS operation used to compute the output differential variance.

conditions at the end of this phase. This filter driven by a noise source $e(t)$ gives an output noise $v_{C_{\text{ref}}}(t)$

$$dv_{C_{\text{ref}}}(t) = -\omega_{\text{eq}} v_{C_{\text{ref}}}(t) \cdot dt + \omega_{\text{eq}} e(t) \cdot dt \tag{5}$$

where ω_{eq} is the cut-off frequency of the first order filter. Then in its convolutional form

$$v_{C_{\text{ref}}}(t) = v_{C_{\text{ref}}}(0) e^{-\omega_{\text{eq}} t} + \omega_{\text{eq}} e^{-\omega_{\text{eq}} t} \int_0^t e^{-\omega_{\text{eq}} u} e(u) \cdot du \tag{6}$$

where the time 0 corresponds to the beginning of the phase T_4, and t the end. The noise level $v_{C_{\rm sig}}(t)$ stored on $C_{\rm sig}$ may be calculated in the same way during the phase T_6 as follows:

$$v_{C_{\rm sig}}(t) = v_{C_{\rm sig}}(0)e^{-\omega_{\rm eq}t} + \omega_{\rm eq}e^{-\omega_{\rm eq}t}\int_0^t e^{-\omega_{\rm eq}w}e(w)\cdot dw \tag{7}$$

In the last expression, 0 and t correspond, respectively, to the beginning and the end of the period T_6 whose duration is the same as T_4.

If $E(v)$ denotes the *expected value* or *mean* of the signal v [24], the variance of $v_{C_{\rm ref}}(t)$, $\sigma^2_{v_{C_{\rm ref}}}(t) = E\{v^2_{C_{\rm ref}}(t)\}$, is given by

$$\begin{aligned} E\left\{v^2_{C_{\rm ref}}(t)\right\} &= E\left\{v^2_{C_{\rm ref}}(0)\right\}\cdot e^{-2\omega_{\rm eq}t} \\ &\quad + \omega^2_{\rm eq}e^{-2\omega_{\rm eq}t}\int_0^t\int_0^t e^{\omega_{\rm eq}x}e^{\omega_{\rm eq}y} \\ &\quad \cdot E\{e(x)\cdot e(y)\}\,dx\cdot dy \end{aligned} \tag{8}$$

where the mute time-variables x and y belong to the time interval T_4.

Remark that, the first term decreases rapidly to 0 and will be neglected for both $v_{C_{\rm ref}}$ and $v_{C_{\rm sig}}$. We obtain an identical expression for $v_{C_{\rm sig}}(t)$ and the same numerical value, as $T_4 = T_6$, assuming that $e(t)$ is a stationary stochastic process

$$E\left\{v^2_{C_{\rm sig}}(t)\right\} = E\left\{v^2_{C_{\rm ref}}(t)\right\}.$$

The cross-correlation is given in the same way by

$$\begin{aligned} &E\{v_{C_{\rm ref}}(t)\cdot v_{C_{\rm sig}}(t)\} \\ &= \omega^2_{\rm eq}e^{-2\omega_{\rm eq}t}\int_0^t\int_0^t e^{\omega_{\rm eq}x}e^{\omega_{\rm eq}y}E\{e(x)\cdot e(y)\}\,dx\cdot dy \end{aligned} \tag{9}$$

where x belongs to the time interval T_4, and y to T_6.

The CDS operation purpose is to get

$$\Delta v_S = v_{C_{\rm ref}} - v_{C_{\rm sig}}$$

whose variance, as $E\{v^2_{C_{\rm sig}}(t)\} = E\{v^2_{C_{\rm ref}}(t)\}$, is given by

$$\begin{aligned} \sigma^2_{\Delta v_S} &= E\left\{\Delta v_S^2\right\} \\ &= 2\left[E\left\{v^2_{C_{\rm ref}}(t)\right\} - E\left\{v_{C_{\rm ref}}(t)\cdot v_{C_{\rm sig}}(t)\right\}\right]. \end{aligned} \tag{10}$$

1) Thermal Noise Input: We recall that, if the single-sided PSD of the white noise input e has the value $a_{\rm th}$, we may write [24]

$$E\{e(x)e(y)\} = \frac{a_{\rm th}}{2}\delta(x-y) \tag{11}$$

where δ denotes the Dirac function. In Fig. 5, if $e(t)$ is a white noise, the cross-correlation given in (9) is zero valued. Actually, x is different from y because they belong to two separate time intervals, and $E\{e(x)\cdot e(y)\} = 0$. Then, from (10)

$$\sigma^2_{\Delta v_S} = 2E\left\{v^2_{C_{\rm ref}}(t)\right\}. \tag{12}$$

As expected, the CDS operation doubles the output white noise power. Using (8), (9) and (10),

$$\sigma^2_{\Delta v_S} = a_{\rm th}\frac{\omega_{\rm eq}}{2}(1 - e^{-2\omega_{\rm eq}\cdot t}) \tag{13}$$

where due to the practical values of t (duration of SHR or SHS signals, >200 ns typically) and $\omega_{\rm eq}$ (100 M radians/s. typically), the exponential term may be neglected. Thus,

$$\sigma^2_{\Delta v_S} = a_{\rm th}\frac{\omega_{\rm eq}}{2} = 2\sigma^2_{v_{C_{\rm ref}}}. \tag{14}$$

2) Flicker Noise Input: In Fig. 5, we suppose now that the input noise is a band-limited flicker noise from f_1 to f_2. The real flicker noise will be obtained by tending f_1 to 0, and f_2 to ∞. According to the Wiener–Kinchine's theorem, the autocorrelation function is the Fourier transform of the double-sided PSD. If the single-sided PSD is given by

$$S_e(f) = \frac{a_{\rm fl}}{|f|}.$$

Then, denoting $\mathrm{Re}(\cdot)$ the real part of $(\cdot)$

$$E\{e(t')e(t'')\} = \mathrm{Re}\left\{\int_{f_1}^{f_2}\frac{a_{\rm fl}}{f}e^{j\omega|t'-t''|}\,d\omega\right\}. \tag{15}$$

If we denote τ the time interval between the phase T_4 and T_6 in the timing diagram ($\tau = T_4 + T_5$), in (9)

$$E\{e(x)e(y)\} = \mathrm{Re}\left\{\int_{f_1}^{f_2}\frac{a_{\rm fl}}{f}e^{j\omega(y+\tau-x)}\,d\omega\right\}. \tag{16}$$

Thus, using (8) and (10), after some calculations, one can find the following expression for the output variance:

$$\begin{aligned} \sigma^2_{\Delta v_S} &= 2\int_{f_1}^{f_2} a_{\rm fl}\frac{\omega^2_{\rm eq}}{\omega} \\ &\quad \cdot\frac{(1+e^{-2\omega_{\rm eq}t} - 2e^{-\omega_{\rm eq}t}\cos(\omega t))(1-\cos(\omega\tau))}{\omega^2_{\rm eq}+\omega^2}\,d\omega. \end{aligned} \tag{17}$$

This integral converges for $f_1 = 0$ and $f_2 = \infty$ and may be rewritten as

$$\begin{aligned} \sigma^2_{\Delta v_S} &= 2\int_0^{\infty} a_{\rm fl}\frac{\omega^2_{\rm eq}}{\omega} \\ &\quad \cdot\frac{(1+e^{-2\omega_{\rm eq}t} - 2e^{-\omega_{\rm eq}t}\cos(\omega t))(1-\cos(\omega\tau))}{\omega^2_{\rm eq}+\omega^2}\,d\omega \end{aligned} \tag{18}$$

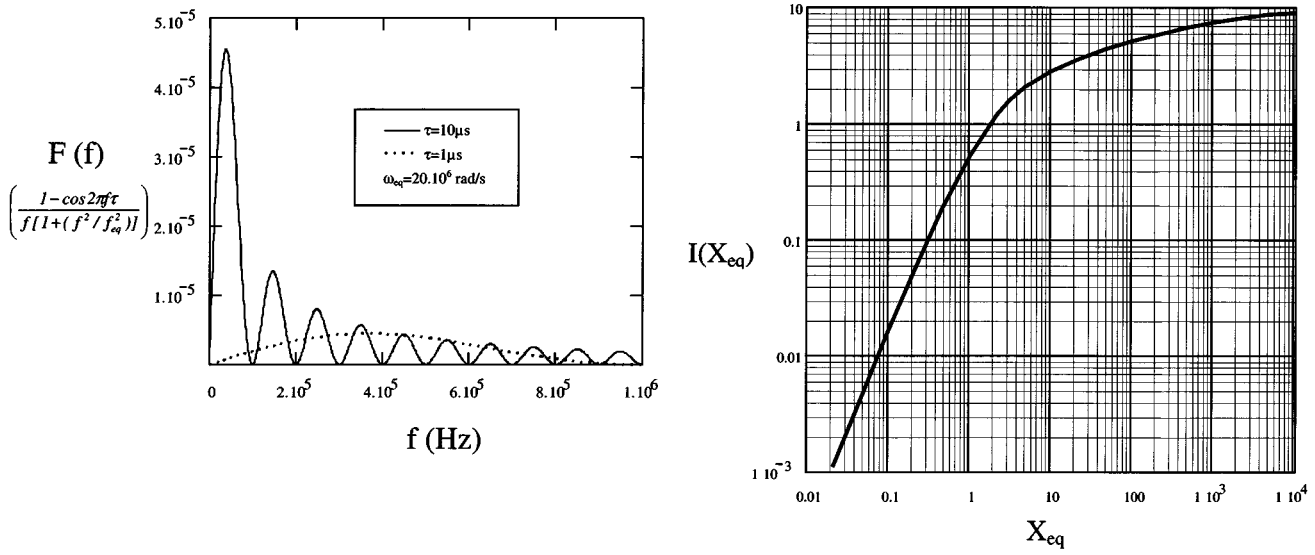
Considering the practical values of $\omega_{\rm eq}$ and t (duration of SHR or SHS signals), and replacing ω by $2\pi f$, this expression may be reduced to

$$\begin{aligned} \sigma^2_{\Delta v_S} &= 2a_{\rm fl}\cdot\int_0^{\infty}\frac{1-\cos 2\pi f\tau}{f(1+(f^2/f^2_{\rm eq}))}\cdot df \\ &= 2a_{\rm fl}\int_0^{\infty}F(f)\cdot df = 2a_{\rm fl}I \end{aligned} \tag{19}$$

where the integral I may be rewritten as

$$I(x_{\rm eq}) = \int_0^{\infty}\frac{1-\cos x}{x(1+(x^2/x^2_{\rm eq}))}\cdot dx \tag{20}$$

with $x_{\rm eq} = 2\pi\tau f_{\rm eq}$. The integral is not singular at $x = 0$. The function $F(f)$ in the integral is plotted in Fig. 6(a). The value of the integral is evaluated numerically and plotted as a function of $x_{\rm eq}$ in Fig. 6(b). The variance of the output signal depends on τ. Note that, the lower the value of τ, the lower the variance and



(a) (b)

Fig. 6. Plot of (a) the function $F(f)$, and (b) the function $I(X_{\rm eq})$ $(X_{\rm eq} = 2\pi f_{\rm eq}\tau)$.

that, for $1/f$ noise, the CDS operation acts like a bandpass filter which eliminates low-frequencies and the singularity at $f = 0$.

B. Contribution of the NMOS Buffer

The NMOS buffer behaves as a first order lowpass system whose output noise PSD is given by

$$S_{v_N} = \frac{R_{\rm eq1}^2 S_{i_{n1}} + r_2^2 S_{i_{n2}} + (r_2 + R_3)^2 S_{i_{n3}} + r_4^2 S_{i_{n4}}}{1 + \left(f^2/f_{\rm eqn}^2\right)}. \tag{21}$$

For the thermal noise, using (14) and (21), the variance of the sampled signal, i.e., the variance of the differential voltage $(v_{C_{\rm ref}} - v_{C_{\rm sig}})$ measured across the sampling capacitors (see Fig. 1) is given by

$$\sigma_{v_N}^2({\rm th}) = \pi f_{\rm eqn}\left[R_{\rm eq1}^2 a_{\rm th1} + r_2^2 a_{\rm th2} + (r_2 + R_{\rm eq1})^2 a_{\rm th3} + r_4^2 a_{\rm th4}\right] \tag{22}$$

in which $a_{\rm th}$ is the *current* thermal noise PSD of the corresponding transistor.

The flicker noises generated by M_4 and M_4' (Fig. 1) are not correlated. Thus the calculations of the Section III-A are not applicable to these transistors[1]. In this case, due to the difficulty in the determination of the lowest limit of the flicker noise, a problem inherent to $1/f$ noise, the computation of flicker noise power is more ticklish. We will assume that the transistor M_4 has reached the steady-state conditions and we use the classical integration of the PSD to obtain the variance. As a general rule, we set the lower limit of the integral to the inverse of the observation time of the signal [25], i.e., $f_{\min 1} = 1/T_4$, where T_4 is the pulse width of SHR or SHS signals. If $S_{\rm in} = a_{\rm fl}/f$ denotes the *current* flicker noise PSD for each transistor, that noise may be computed as

$$\sigma_{M_4}^2({\rm fl}) = r_4^2 a_{\rm fl4} \cdot \int_{f_{\min 1}}^{\infty} \frac{1}{f(1 + (f^2/f_{\rm eqn}^2))} \cdot df = \frac{1}{2} r_4^2 a_{\rm fl4} \ln\left(1 + \frac{f_{\rm eqn}^2}{f_{\min 1}^2}\right) \tag{23}$$

and the total $1/f$ noise power, using (19)

$$\sigma_{v_N}^2({\rm fl}) = 2I \cdot \left[R_{\rm eq1}^2 a_{\rm fl1} + r_2^2 a_{\rm fl2} + (r_2 + R_{\rm eq1})^2 a_{\rm fl3}\right] + 2\sigma_{M_4}^2({\rm fl}) \tag{24}$$

Note that, as the total noise of the readout circuit is strongly dominated by other noise sources, we couldn't verify this lowest limit assumption for M_4 experimentally.

C. Contribution of the PMOS Buffers

The outputs of the two PMOS buffers are sampled separately. Thus the total thermal noise contribution of these buffers may be calculated from (4) by multiplying the variance of one of them by two:

$$\sigma_{v_P}^2({\rm th}) = \pi f_{\rm eq1P}\left[R_{\rm eq2}^2 a_{\rm th5} + r_6^2 a_{\rm th6} + (r_6 + R_{\rm eq2})^2 a_{\rm th7}\right] \tag{25}$$

in which $a_{\rm th}$ is the *current* thermal noise PSD of the corresponding transistor.

As output signals are sampled once using separate buffers, in opposition to the flicker noise of NMOS buffers, the CDS operation do not reduce the flicker noise of the PMOS buffers. By using the method already used to calculate the flicker noise of M_4 in the previous section, and setting the lower limit of the integral to $f_{\min 2} = 1/T_8$, the output variance is

$$\sigma_{v_P}^2({\rm fl}) = 2\left[R_{\rm eq2}^2 a_{\rm fl5} + r_6^2 a_{\rm fl6} + (r_6 + R_{\rm eq2})^2 a_{\rm fl7}\right] \cdot \int_{f_{\min 2}}^{\infty} \frac{1}{f(1 + (f^2/f_{\rm eq1P}^2))} \cdot df \tag{26}$$

[1]The noise contribution of the switch configured transistors M_4-M_4' is often assumed to be negligible in the literature [5], [6]; however its contribution is taken into account here to confirm this assumption.

and

$$\sigma^2_{v_P}(\mathrm{fl}) = \left\{\ln\left(1+\frac{f^2_{\mathrm{eq}P}}{f^2_{\min 2}}\right)\right\} \cdot \left[R^2_{\mathrm{eq}2}a_{\mathrm{fl}5} + r^2_6 a_{\mathrm{fl}6} + (r_6+R_{\mathrm{eq}2})^2 a_{\mathrm{fl}7}\right]. \quad (27)$$

D. Contribution of the Reset Transistor

From the Fig. 3, one can see that a capacitive positive feedback is formed by the capacitors C_{fd} and $C_{\mathrm{gs}1}$. An *effective sense capacitance* C_{eff} may be defined as [20], [5]

$$C_{\mathrm{eff}} = C_{fd} + (1-A'_1)C_{\mathrm{gs}1} \quad (28)$$

where A'_1 is the dc gain from the gate to source terminals of M_1. The expression for A'_1 is given in Appendix B.

At the end of the RST pulse (T_1 in Fig. 1(b)), the drain current flowing into the transistor M_{RST} reduces to the drain-bulk leakage current and the current flowing from the inversion layer to the bulk [22]. Thus, the effective sense capacitance C_{eff} is charged through a transistor being in weak inversion (subthreshold region).

The interpretation of the white noise generated by the MOS transistor in weak inversion is also subject of controversy in the literature, and may be seen as "shot noise" or "thermal noise" [26], [22]. A unified white noise model for the MOS transistor at the subthreshold region is presented in [27]. It has been shown that [27], in thermal equilibrium considering fixed gate and drain voltages, the noise charged into a capacitor C via a MOSFET at the subthreshold region is always equal to

$$\sigma^2 = \frac{kT}{C} \quad (29)$$

which is the familiar expression of the noise of the reset transistor M_{RST} [28]. Then the reset noise expression may be given as:

$$\sigma^2_{\mathrm{RESET}} = \frac{kT}{C_{\mathrm{eff}}} \quad (30)$$

As we will see in the Section VII, this expression is verified experimentally.

As this study is emphasized on photogate type pixels (Fig. 1), where the kT/C noise is eliminated[2] by CDS operation, we do not investigate this noise further here. The flicker noise contribution of M_{RST} is eliminated by the CDS operation as well as the kT/C noise.

E. Total Output Differential and Input Referred Noise with CDS

The total variance of the output differential signal may be expressed as:

$$\sigma^2_{v_o}(\mathrm{tot}) = A_2^2\sigma^2_{v_N}(\mathrm{th}) + A_2^2\sigma^2_{v_N}(\mathrm{fl}) + \sigma^2_{v_P}(\mathrm{th}) + \sigma^2_{v_P}(\mathrm{fl}) \quad (31)$$

A_1 and A_2 denote, respectively, the dc gain of the NMOS buffer and PMOS buffer. The analytical expressions for A_1 and A_2 are given in Appendix B.

[2]Due to the nonlinearity of the floating node capacitance, there is a residual kT/C noise after CDS but its contribution on the total noise standard deviation is negligible (less than 2% for the photogate pixel).

Note that, in the standard three transistors photodiode pixel case [2], the noise $\sigma^2_{\mathrm{RESET}}$ expression of reset transistor also must be added to the right side of the output noise expression (31) as

$$\sigma^2_{\mathrm{RESET}} = A_1^2A_2^2\frac{2kT}{C_{\mathrm{eff}}}. \quad (32)$$

The factor of two is due to the double sampling, uncorrelated in this case.

The total input referred noise in volts is

$$\sigma_{v_i}(\mathrm{tot}) = \frac{\sqrt{\sigma^2_{v_o}(\mathrm{tot})}}{A_1A_2}. \quad (33)$$

The input referred noise for a CMOS active pixel sensor can be expressed as the equivalent number of electrons at the sense node that produces a voltage at the output equal to the noise voltage resulting from all the noise sources in the signal chain [5], i.e.,

$$\mathrm{NEQ} = \frac{\sqrt{\sigma^2_{v_o}(\mathrm{tot})}}{\mathrm{CVF}} \quad (\mathrm{e}^-) \quad (34)$$

where CVF is the charge-to-voltage conversion gain (V/electron) from the sense node to output:

$$\mathrm{CVF} = A_1A_2\frac{q_{\mathrm{elec}}}{C_{\mathrm{eff}}} \quad (35)$$

in which $q_{\mathrm{elec}} = 1,6\cdot 10^{-19}$ [C/electron] the elementary charge.

IV. Analysis of the Output RMS Noise Without CDS Operation

In this case, we consider a single sampling of the signal and a single output, i.e., only one of the signal paths in Fig. 1(a) is used. In this case, the total variance of the output signal may be expressed as

$$\sigma^2_{vo}(\mathrm{tot}) = \frac{1}{2}\left\{A_2^2\sigma^2_{v_N}(\mathrm{th}) + A_2^2\tilde{\sigma}^2_{v_N}(\mathrm{fl}) + \sigma^2_{v_P}(\mathrm{th}) + \sigma^2_{v_P}(\mathrm{fl}) + \sigma^2_{\mathrm{RESET}}\right\} \quad (36)$$

where $\tilde{\sigma}^2_{v_N}(\mathrm{fl})$ is defined as follows:

$$\tilde{\sigma}^2_{v_N}(\mathrm{fl}) = \left\{\ln\left(1+\frac{f^2_{\mathrm{eq}n}}{f^2_{\min 1}}\right)\right\} \cdot \left[R^2_{\mathrm{eq}1}a_{\mathrm{fl}1} + r_2^2 a_{\mathrm{fl}2} + (r_2+R_{\mathrm{eq}1})^2 a_{\mathrm{fl}3} + r_4^2 a_{\mathrm{fl}4}\right] \quad (37)$$

in which a_{fl} is the *current* flicker noise PSD coefficient ($S_{\mathrm{in}} = a_{\mathrm{fl}}/f$) of each transistor and $f_{\min 1} = 1/T_4$. T_4 is the pulse width of sampling signal SHR [see Fig. 1(b)]. The other terms in (36) are defined in the previous section.

V. Simulation-Oriented MOSFET Noise Models

In this section, we will survey briefly the available simulation-oriented thermal and flicker noise models for the MOS transistor. There are several simulation-oriented thermal and flicker noise models proposed in literature, considering all operating regions and inversion levels. However, as we will see, most of them are valid only for long-channel devices and need physical parameters rarely provided by silicon foundries.

We will consider the common small-signal equivalent circuit of the MOS transistor, shown in Fig. 2.

1) Thermal Noise Models: The thermal noise models used in SPICE2 and those given in [29]–[32] are based on the model given in [33] and implemented in circuit simulators as

$$S_{\rm ind} = \gamma 4kTg_{\rm tot} \tag{38}$$

where $g_{\rm tot} = g_m$ or $g_{\rm tot} = g_m + g_{mb} + g_{\rm ds}$, and γ is a bias-dependent device parameter. γ equals one at zero drain bias, and $2/3$ at saturation. Nevertheless, in these models, the effects of the drain and the source electric fields on the bulk charge and inversion charge under the oxide are neglected, and they are valid only for long-channel devices. For short-channel devices, this expression gives often optimistic noise results and significant deviations were observed from this equation [34], [21].

The most general form of the thermal noise in MOS transistors is given by the relation [35]

$$S_{\rm ind} = 4kT\frac{\mu}{L^2}|Q_{\rm inv}| \tag{39}$$

where $Q_{\rm inv}$ the inversion channel charge. If the appropriate expression is used for $Q_{\rm inv}$, this equation is valid for all operating regions [22]. A thermal noise model based on (39), which takes into account short-channel effects, and valid both at weak and strong inversion is developed in [34] by developing analytically the value of $Q_{\rm inv}$ and implemented in some circuit simulators.

In (39), replacing μ by the effective surface mobility $\mu_{\rm eff}$ to include mobility degradation, and L by $L_{\rm eff}$ effective channel length to include channel length modulation leads to

$$S_{\rm ind} = 4kT\frac{\mu_{\rm eff}}{L_{\rm eff}^2}|Q_{\rm inv}|. \tag{40}$$

A thermal noise model based on this equation, taking into account short-channel effects, valid at the ohmic and saturation regions, is developed by calculating $Q_{\rm inv}$ in [36]. Equation (40) is used as a thermal noise model in the BSIM3 (Berkeley Short-channel IGFET Model) [37]. It is also implemented in the recent revisions of the EKV (Enz–Krummenacher–Vittoz) model [38], [39], in a slightly modified form.

Some other thermal noise sources in MOS transistors not considered in circuit simulators are induced gate noise [33], the noise generated by the substrate current, the noise generated by the gate resistance for large gate-area devices, and the noise generated by the substrate resistance [40]. The effects of the substrate resistance and the gate resistance are important in HF applications [40], [41]. The noise generated by the substrate current may become important for transistors with very small geometries [22].

2) Flicker Noise Models: Simulation-oriented flicker noise models given in literature for MOSFET's are in general semi-empirical or entirely empirical. The flicker noise model often found in circuit simulators (SPICE2) is the entirely empirical relation

$$S_{\rm ind} = \frac{K_F \cdot I_{\rm ds}^{AF}}{C_{\rm ox}L_{\rm eff}^2 f^{EF}} \tag{41}$$

where K_F, AF, and EF are empirical parameters supplied by the silicon foundry. EF is very close to unity. It is valid only in strong inversion, and has some problems in representing the noise behavior of transistors as a function of channel areas [21], [42].

A model based on the number fluctuation model [43], [44], valid only for long-channel devices, implemented in circuit simulators is

$$S_{\rm ind} = \frac{K_F \cdot g_m^2}{C_{\rm ox}^2 W_{\rm eff} \cdot L_{\rm eff} \cdot f^{AF}} \tag{42}$$

where K_F and AF are empirical parameters, different from those used in (41). This model is valid from weak inversion to strong inversion, provided that a coefficient which is the ratio of the fluctuations in carrier number to fluctuations in occupied trap number is used. The value of this coefficient is close to unity at strong inversion, and decreases significantly at weak inversion [43]. Nevertheless, in circuit simulators, a constant K_F parameter is often used, making the model only valid in strong inversion.

BSIM3 provides a physics-based unified flicker noise model developed in [45], [46] valid both in weak and strong inversion operating regions, and taking into account short-channel effects. It is based on both oxide trap-induced carrier number and surface mobility fluctuations. In strong inversion, the drain current noise density is given [37] by (43), shown at the bottom of the page, where V_t is the thermal voltage, and $\Delta L_{\rm clm}$ the channel length reduction due to channel length modulation. N_o and N_l are, respectively, the charge density at the source and drain ends. $NOI\,A, NOI\,B$, and $NOI\,C$ are empirical parameters. In the linear operating region, the second term is zero valued. The relations for $N_o, N_l, \Delta L_{\rm clm}$, in the weak inversion region can be found in [37], and will not be repeated here. The empirical parameters are not always provided by the foundries, and the low-frequency noise simulations using the default values of these parameters often give unrealistic results [47], [48].

VI. Test Structures and the Experimental Set-Up

To validate the analytical expressions, and examine the influence of the transistor and capacitor sizes on the output noise, test structures have been realized. The microphotograph of the test chip fabricated using a *Alcatel Microelectronics* 0.7 μm CMOS

$$S_{\rm ind} = \frac{q^2 V_t \mu_{\rm eff} I_{\rm ds}}{C_{\rm ox}L_{\rm eff}^2 f^{EF} \cdot 10^8}\left\{NOI\,A \cdot \ln\left(\frac{N_o + 2\cdot 10^{14}}{N_l + 2\cdot 10^{14}}\right) + NOI\,B(N_o - N_l) + \frac{NOI\,C}{2}\left(N_o^2 - N_l^2\right)\right\} + \frac{V_t I_{\rm ds}^2 \Delta L_{\rm clm}}{W_{\rm eff}L_{\rm eff}^2 f^{EF} \cdot 10^8} \cdot \frac{NOI\,A + NOI\,B \cdot N_l + NOI\,C \cdot N_l^2}{(N_l + 2\cdot 10^{14})^2} \tag{43}$$

TABLE I
TRANSISTOR AND CAPACITOR SIZES FOR THE TEST CIRCUITS

Test Circuit	M_{RST} (W/L)	C_{fd} (fF)	M_1 (W/L)	M_2 (W/L)	M_3 (W/L)	M4 (W/L)	C_{SH} (pF)
1	2.2μm/0.7μm	15	1.1μm/0.7μm	2.2μm/0.7μm	4.4μm/4.9μm	2.2μm/0.7μm	1.2
2		15	2.2μm/0.7μm		4.4μm/4.9μm		
3		15	6.0μm/0.7μm		4.4μm/4.9μm		
4		15	15μm/0.7μm		4.4μm/4.9μm		
5		15	2.2μm/0.7μm		1.0μm/4.9μm		
6		15	2.2μm/0.7μm		2.2μm/4.9μm		
7		5	2.2μm/0.7μm		4.4μm/4.9μm		
8		28	2.2μm/0.7μm		4.4μm/4.9μm		

$I_{bias\_NMOS\_Buffer}$=30μA, $I_{bias\_PMOS\_Buffer}$=120μA

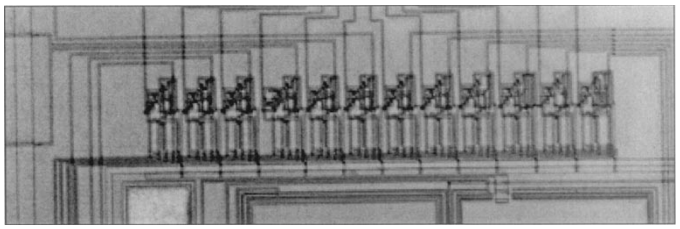


Fig. 7. Microphotograph of the test chip.

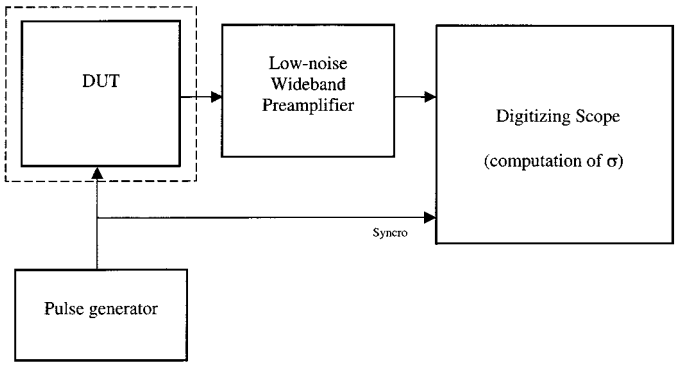


Fig. 8. Experimental set-up used to measure the output rms noise.

technology available through *EUROPRACTICE* MPW service, is shown in Fig. 7.

The test circuit is given in Fig. 1(a). To distinguish between in-pixel noise sources and the readout circuit noise, the floating node capacitance only is included in the test structures; the charge transfer transistor TX and the photosensitive MOS capacitor PG, are not implemented.

The number of test circuits is limited by the large number of I/O pads required. In the test structures, different values for W_1, W_3 channel widths and C_{fd} are considered (Table I).

The experimental test bench for the rms noise measurements is shown in Fig. 8. It consists of an *EG&G 5185* low-noise preamplifier, a pulse generator, and a numerical scope. The scope is able to compute the variance of the samples directly. The whole system is located in a Faraday cage. All measurements were made at room temperature and in darkness conditions. The results are corrected from noise of the test bench. 300 samples were taken for each point of measure. $T_1 = T_4 = T_6 = 200$ ns, and $T_5 = 1.5$ μs [Fig. 1(b)].

VII. RESULTS AND DISCUSSION

In all the figures, unless otherwise stated, the thermal noise is calculated using (40), and the flicker noise using (41).

All the parameters required for noise computations (transistor terminal voltages, currents, transconductances, capacitances, terminal charges, effective channel dimensions, etc.) are extracted from the ELDO circuit simulator [49], following a dc point simulation of the circuit given in Fig. 1(a). The physical parameters and the dc gains of the buffers A_1, A_1' and A_2 (see Appendix B) depend on the operating point of the transistors and are computed for each input parameter value.

The inversion charge $Q_{\rm inv}$ needed for (40) is defined as

$$|Q_{\rm inv}| = |Q_D + Q_S| \tag{44}$$

where Q_D and Q_S are, respectively, charges associated with the drain and source terminals [37], [22]. $Q_{\rm inv}$ is calculated by extracting Q_D and Q_S from the circuit simulator. The relations used to compute the effective mobility $\mu_{\rm eff}$ may be found in [37], and are not repeated here.

The experimental and theoretical expected output rms noise, and input referred noise are plotted, respectively, in Figs. 9(a) and (b), as a function of the source follower M_1 channel width W_1 with CDS operation. The channel length L_1 is kept constant. It is verified that, for a given W/L, each transistor in the test circuits is in appropriate operating region, i.e., M_1 and M_3 are saturated, M_2 in the ohmic region, both in strong inversion.

In this figure, the total thermal noise calculated using the SPICE2 thermal noise model given in (38) with $\gamma = 2/3$, and the total flicker noise contribution based on BSIM3 flicker noise models (43), are also included. The empirical flicker noise parameters $NOIA, NOIB$, and $NOIC$ are not supplied by our foundry, and the flicker noise is calculated using the default values to give only qualitative behavior. It should be noted that the classical SPICE2 thermal noise model fails and gives lower thermal noise level.

It is also interesting to remark that, the empirical flicker noise equation (41) gives incorrectly the same $1/f$ noise densities for M_1 and M_2 which are at different operating regions (not illustrated in the Fig. 9), on the contrary of BSIM3 flicker noise models.

While the increase of W_1 rises the thermal noise density (and reduces $1/f$ noise density), it decreases the dynamic output resistance $R_{\rm eq1}$ of M_1 seen from its source terminal. Thus, there is an optimum channel width $W_{\rm opt}$ which gives a minimum input

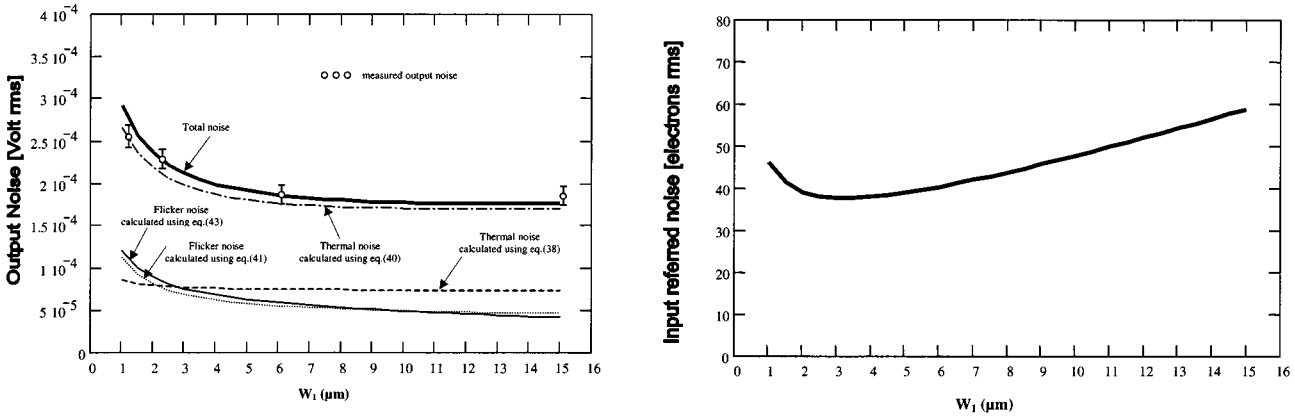


Fig. 9. Total output and input referred rms noise as a function of the in-pixel source follower M_1 channel width, with CDS operation ($L_1 = 0.7\ \mu$m, $I_{\text{bias_NMOS}} = 30\ \mu$A, $I_{\text{bias_PMOS}} = 120\ \mu$A).

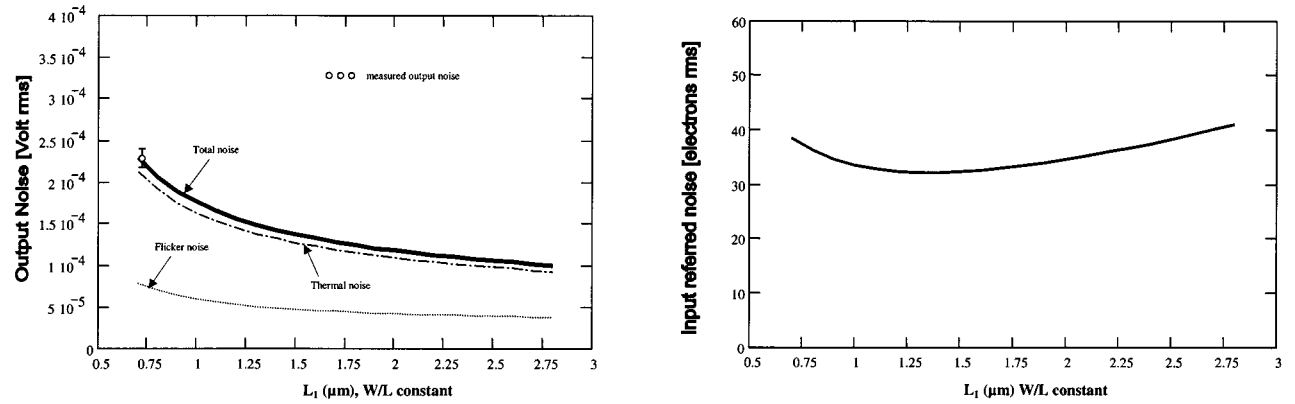


Fig. 10. Total output and input referred rms noise as a function of the channel length L_1 of the source follower M_1, with CDS operation. The aspect ratio W_1/L_1 is kept constant. ($I_{\text{bias_NMOS}} = 30\ \mu$A, $I_{\text{bias_PMOS}} = 120\ \mu$A).

referred noise. Beyond this value, a further increase of W_1 does not reduce the noise. At very low channel width values, both thermal noise and flicker noise become important, principally due to R_{eq1}.

Fig. 10 shows the rms noise as a function of source follower channel length L_1, keeping the aspect ratio W_1/L_1 constant. For very small L_1 values, due to the decreased source-to-gate capacitance of M_1, the input referred noise increases. Thus, an optimum value of $(W_1 \times L_1)$ also exist.

The output noise as a function of the bias current of the NMOS buffer is shown in Fig. 11. The biasing current is adjusted by V_{LN}. Both theoretical and experimental results show that the larger the bias current, the lower the output and input referred noise. The increase of I_{bias} increases the transconductance of M_1, which decreases the R_{eq1}. The dimensions of the load transistor M_3 have a weak[3] effect on the noise level, and only fixes the bias current of the NMOS buffer.

The total rms noise as a function of the effective sense node capacitance C_{eff} is given in Fig. 12. It is obvious that the increase of C_{eff} decreases the charge-to-voltage conversion factor CVF [see (32)], and the input referred noise rises.

[3]Actually, this transistor, external to the pixel, is customarily designed with a large channel length (see Table I); so its noise contribution is very small compared with M_1. Our simulations show that its contribution becomes nonnegligible only for short channel lengths ($L_3 < 1.5\ \mu$m).

The effect of the size of C_S capacitors (C_{ref} and C_{sig}) is obvious from (1). The results are given in Fig. 13. The reduction of the channel width of the switch M_4, and the enlargement of the size of the capacitor C_S reduce the bandwidth of the system and the noise, reducing the output rms thermal noise. Another advantage of the latter, is the decrease of the clock feedthrough effects [50].

Fig. 14 shows the rms noise as a function of the floating node capacitance C_{eff} observed at one of the outputs, without CDS operation. The measured output noise value is slightly higher than kT/C_{eff}, due to the contributions of the thermal noise and flicker noise of the readout chain.

VIII. Conclusion

A detailed analytical noise analysis of the CMOS image sensor signal acquisition chain is presented, considering both the thermal noise and low-frequency noise sources. The CDS operation is also considered. A good agreement was observed between experimental and analytical results, using (40) for thermal noise. The classical SPICE2 thermal noise model (38) significantly underestimate the noise level.

For the photogate pixel after the CDS operation, in most cases, the dominant noise source is the thermal noise generated by the in-pixel source follower transistor M_1 [Fig. 1(a)]. CDS

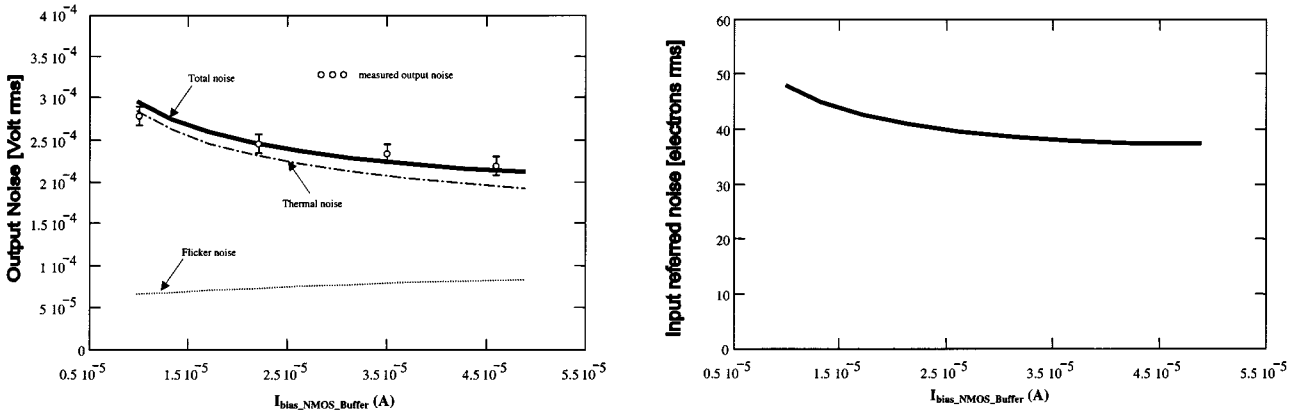


Fig. 11. Total output and input referred rms noise as a function of the in-pixel NMOS buffer bias current, with CDS operation (test circuit no. 2, see Table I, $I_{\rm bias_PMOS} = 120\ \mu$A).

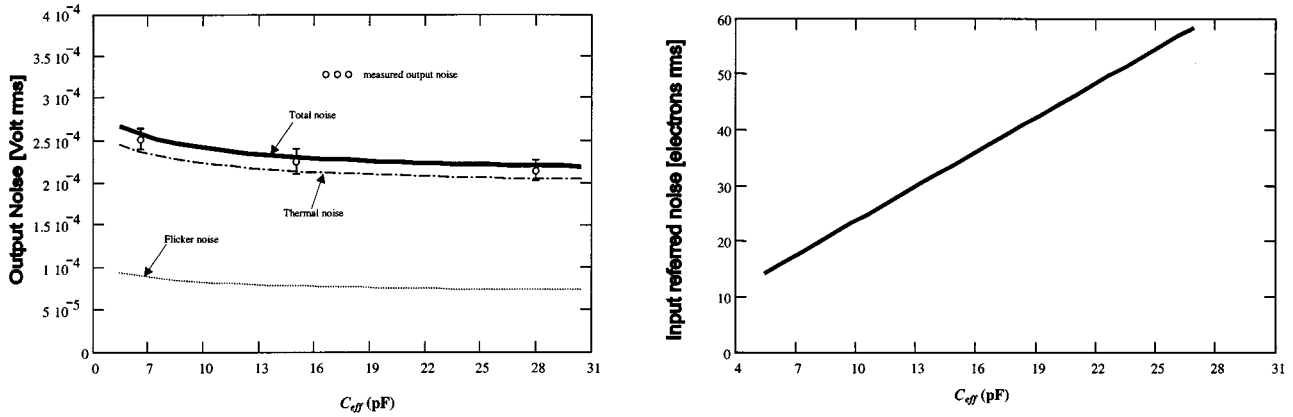


Fig. 12. Total output and input referred rms noise as a function of the floating node capacitance $C_{\rm eff}$, with CDS operation ($I_{\rm bias_NMOS} = 30\ \mu$A, $I_{\rm bias_PMOS} = 120\ \mu$A).

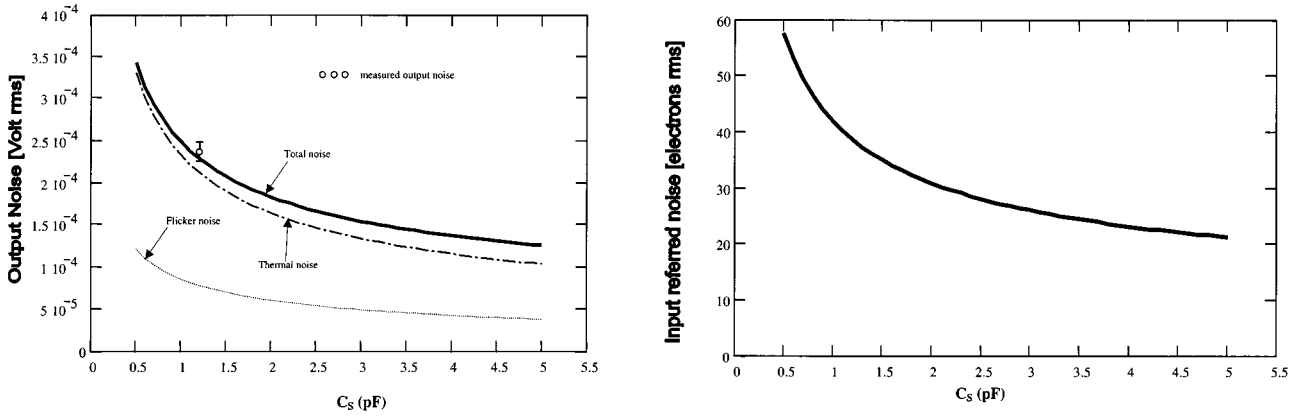


Fig. 13. Total output and input referred rms noise as a function of the sampling capacitor C_S ($C_{\rm ref}$ or $C_{\rm sig}$), with CDS operation ($I_{\rm bias_NMOS} = 30\ \mu$A, $I_{\rm bias_PMOS} = 120\ \mu$A).

operation doubles the thermal noise power. Flicker noise is less significant than the thermal noise. Nevertheless, for very small geometry transistors, flicker noise also become important.

The channel width and length optimums for the source follower transistor M_1 is slightly above the minimum process determined channel width and length. Above these values, larger input transistor area and aspect ratio give larger input referred noise.

The total noise depends also strongly on the bias current of the in-pixel NMOS buffer. For lower noise, the bias current must be as large as possible, to the detriment of the maximum power consumption specification of the device. A tradeoff has to be found depending on the application.

The floating diffusion node capacitance must be reduced to minimize the input referred noise, but this may degrade the charge handling capacity of the pixel in the context of low-voltage operation.

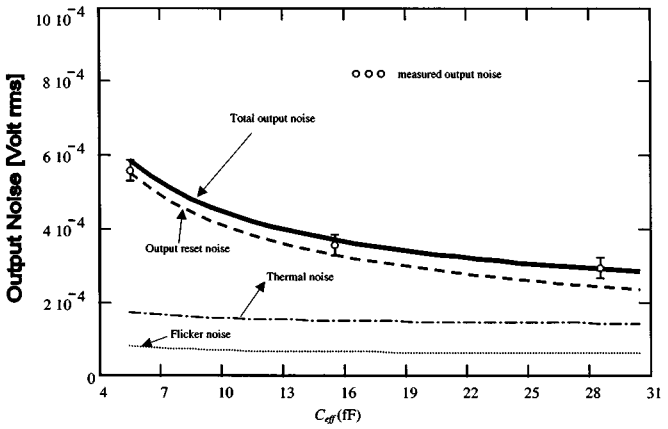


Fig. 14. Output rms noise as a function of the floating node capacitance $C_{\rm eff}$ observed at one of the outputs, without CDS operation ($I_{\rm bias_NMOS} = 30\ \mu$A, $I_{\rm bias_PMOS} = 120\ \mu$A).

To reduce the thermal noise, the sampling capacitances, $C_{\rm ref}$ and $C_{\rm sig}$, must be as large as possible, which reduces both the signal and the noise bandwidths. Of course, the increase of C_S limits the readout speed. However, unlike the CCD's [51], in CMOS active pixel sensors the speed of the NMOS buffer is a less important criterion, because the main limiting factor is the scanning speed of the imager columns.

APPENDIX A
NOISE OF IN-PIXEL NMOS BUFFER STORED ON THE SAMPLING CAPACITOR

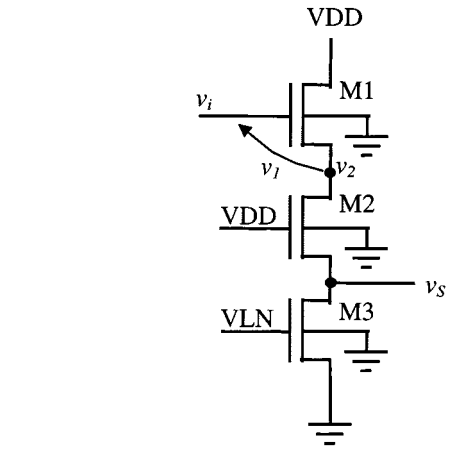
A nodal analysis of the equivalent circuit of Fig. 3(b) leads to the relation (A1), shown at the bottom of the page, with

$$R_{\rm eq1} = [g_{mb1} + g_{m1}\frac{C_{fd}}{C_{fd}+C_{\rm gs1}}]^{-1}$$

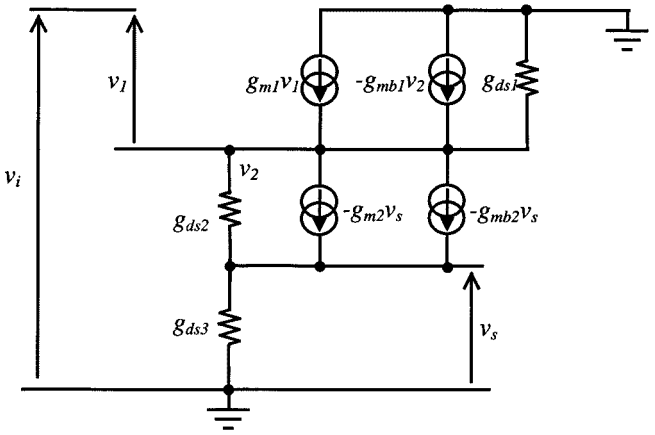
and

$$C_{\rm eq1} = \frac{C_{\rm gs1}C_{fd}}{C_{\rm gs1}+C_{fd}}.$$

$R_{\rm eq1}$ is the dynamic output resistance of M_1 seen from its source terminal and $C_{\rm eq1}$ the output equivalent capacitance of M_1 seen between its source and the ground. This transfer function is difficult to handle analytically, thus it must be simplified by doing some assumptions. The typical values are $R_{\rm eq1} \approx 10$ kΩ, $C_{\rm eq1} \approx 5$ fF, $C_S \approx 1$ pF, $R_3 \approx 1$ MΩ, $r_2 \approx 1$ k, $r_4 \approx 1$ k. Thus, $R_3 > r_2, R_3 > R_{\rm eq1}$ and $R_{\rm eq1}C_{\rm eq1} \ll R_3C_S$. In addition, at the working frequencies, assuming that $f \ll 10^9$ Hz,



(a)



(b)

Fig. 15. (a) In-pixel source follower, and (b) its small-signal equivalent circuit for dc gain calculation.

$R_{\rm eq1}C_{\rm eq1}\omega \ll 1$ is verified. In this case, the transfer function may be reduced to the following first order transfer function

$$v_N = \frac{R_{\rm eq1}i_{n1} + e_{n2} + (r_2 + R_{\rm eq1})i_{n3} + e_{n4}}{1 + j(\omega/\omega_{\rm eqn})} \qquad \text{(A.2)}$$

with

$$\omega_{\rm eqn} = \left[C_S\left(r_4 + \frac{R_3(R_{\rm eq1}+r_2)}{R_3+R_{\rm eq1}+r_2}\right)\right]^{-1}.$$

Due to the fact that the capacitances C_{fd} and $C_{\rm gs1}$ are negligible when compared to C_S, we remark that the filtering process of the noise is only effective when the sampling switch M_4 is active.

$$v_N = \left[e_{n2} + e_{n4}\left(1+\frac{r_2}{R_3}\right) + r_2 i_{n3} + R_{\rm eq1}\left(i_{n1}+i_{n3}+\frac{e_{n4}}{R_3}\right)\right] \cdot \frac{1 + j\frac{R_{\rm eq1}C_{\rm eq1}\omega(R_3+r_2)}{R_3+R_{\rm eq1}+r_2}}{1 + j\omega\left\{C_{\rm eq1}\frac{R_{\rm eq1}(R_3+r_2)}{R_3+R_{\rm eq1}+r_2} + C_S r_4 + \frac{C_S R_3(r_2+R_{\rm eq1})}{R_3+R_{\rm eq1}+r_2}\right\} + (j\omega)^2 C_S C_{\rm eq1} R_{\rm eq1}\left\{\frac{(R_3+r_2)r_4+R_3r_2}{R_3+R_{\rm eq1}+r_2}\right\}} \qquad \text{(A.1)}$$

It should be pointed out that, there is also a parasitic capacitance C_p between the source terminal of M_2 and the ground, due to the wiring and C_{sb}-C_{sg} capacitances of the turned-off M_2 transistors of the other rows, connected to the same common node. For large size arrays, this capacitance become important and should be added in parallel to R_3 in Fig. 3(b). In this case, in (A.1), R_3 should be replaced by $[R_3/(1+j\omega R_3 C_p)]$. Note that, the effect of this capacitance is to improve the noise performance, by reducing the (noise and signal) bandwidth. Thus, our results may be seen as the worst case for noise performance.

APPENDIX B
DC GAIN OF THE BUFFERS

The small-signal equivalent circuit of the NMOS buffer used to calculate the dc gain more accurately is shown in Fig. 15. The g_m and g_{mb} parameters of M_2 are taken into account. The dc gain of the circuit is given by

$$A_1 = \left.\frac{v_S}{v_i}\right|_{\omega=0} = g_{m1}\cdot\left[\frac{1}{g_{\mathrm{ds}2}}(g_{m1}+g_{mb1}+g_{\mathrm{ds}1}) \cdot (g_{m2}+g_{mb2}+g_{\mathrm{ds}2}+g_{\mathrm{ds}3})+g_{\mathrm{ds}3}\right]^{-1} \quad \text{(A.3)}$$

and

$$A_1' = \left.\frac{v_2}{v_i}\right|_{\omega=0} = A_1\cdot\left[1+\frac{g_{m2}+g_{mb2}+g_{\mathrm{ds}3}}{g_{\mathrm{ds}2}}\right]. \quad \text{(A.4)}$$

In the same way, the gain of the PMOS buffer may be calculated readily, which leads to

$$A_2 = g_{m5}\cdot\left[\frac{1}{g_{\mathrm{ds}6}}(g_{m5}+g_{mb5}+g_{\mathrm{ds}5}) \cdot (g_{m6}+g_{mb6}+g_{\mathrm{ds}6}+g_{\mathrm{ds}7})+g_{\mathrm{ds}7}\right]^{-1}. \quad \text{(A.5)}$$

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